Thermal stress analysis of wafer-level multilayer stacking process for 3D-TSV packaging

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2022 23rd International Conference on Electronic Packaging Technology (ICEPT) | 978-1-6654-9905-7/22/$31.00 ©2022 IEEE | DOI: 10.1109/ICEPT56209.2022.9873205

***Abstract*—Through silicon via (TSV) and stacked bonding are the core technologies to perform vertical interconnect for 3D integration. For wafer-level multilayer stacking process, thermal stress is generated and accumulated due to the difference in thermal expansion coefficients of materials in each layer of the structure. Due to the large thermal stress, the issue of failures in the stacking process are caused by solder joints almost. Hence, thermal stress analyses for multilayer stacking process are in urgent need. In this paper, a finite element model (FEM) is established to investigate the reliabilities for six layered TSV wafer bonded. Selected the General Plane Deformation (GPD) FEM model as the simulation model for conserving computer resources and time because of the large number of TSVs. Birth and death element technology is applied, and descripted the procedure during the six layered wafer staking process. Considered three kinds of solder joint materials for SAC305, Sn63Pb37 and Sn10Pb90, and analyzed the von Mises stress and equivalent plastic strain.**

Keywords—Multilayer stacking; Birth and death element; 3D-TSV packaging

I. INTRODUCTION

With the increasing demand for smaller and more functional electronic products for consumers, and the fierce competition from the merchants of electronic products, traditional planar 2D packaging faces increasingly severe challenges. 3D TSV packaging enables to perform vertical interconnect achieve using bump and TSV technology, and gradually become the focus of attention [1]. It has the advantages of high performance, low power consumption, high bandwidth and low signal delay, which connect various materials and functional devices together to form a highly integrated system through vertical stacking[2]. Due to the difference of thermal expansion coefficient, thermal stress is generated in multilayer stacking process, so the reliability of thermal stress become the focus of research[3, 4]. The issue of failures in the stacking process are caused by solder joints almost, which are generally utilized as main interconnected materials[5]. Therefore, the stress and strain analysis of solder joints is vital important for reliability of the wafer staking process for 3D-TSV packaging.

HAN[6] simulated the bonding process of two-layer chips for different structural parameters used COMSOL software, and evaluated the reliability of the bonding process. Cheng[7] investigated the 3-D TSV packaging, and found that the position of the maximum displacement is at the corner TSV copper bump. Due to misalignment of stacked chips, shear deformation has a significant effect on copper interconnects. Wafer-level warpage and the reliability of TSV-cu in 3D-TSV package structures were investigated [8, 9]. However, the simulations of wafer-level bonding processes are rarely reported. During the stacking process, the plastic deformation, creep and even fracture are generated due to the influence of temperature load. And a large interfacial shear stress is generated at the interface of the solder joint, which further leads to cracking and delamination of the interface.

In this paper, the 3D-TSV stacking process is simulated using the birth and death element technology[10]. Due to the large number of TSVs, the General Plane Deformation (GPD) [11,12] FEM model include six layer was chosen as the simulation model for conserving computer resources and time. Then, The setting of birth and death element corresponding to the process are described in detail. Finally, Considered three kinds of solder joint materials for SAC305, Sn63Pb37 and Sn10Pb90, and analyzed the von Mises stress and equivalent plastic strain. It provides theoretical guidance for studying the reliability of solder joints after the stacking process.

II. MODELLING PROCESS

A. Structure and simplifyed model

A finite element model for six layered 8-inch TSV wafer is established. The size of a single chip is 19.5mm×19.5mm, and the number of TSVs on each chip is 1820. A quarter of the wafer and single chip models of TSVs are shown in Fig.1(a), and a sectional view of the wafer is shown in

Fig.1(b). The seed layer is ignored. The diameter of the TSV is 30μm, the diameter of the Cu pads is 80μm, and the height of the Si is 200μm.

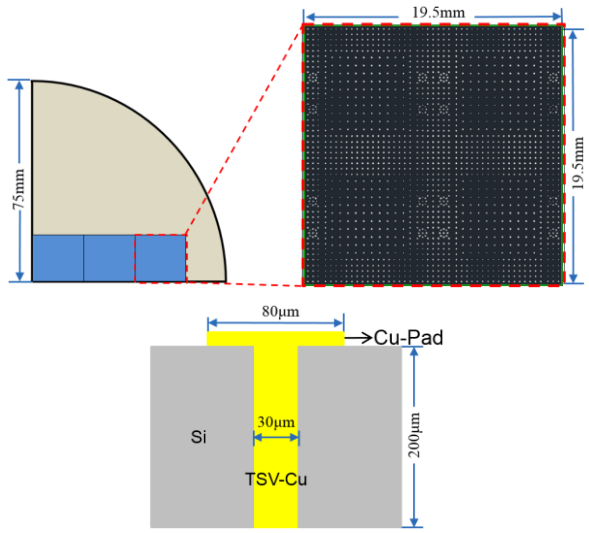

Fig. 1. The structure distribution diagram of wafer.
(a) quarter wafer and single chip (b) sectional view

For the wafer-level finite element model, there is a huge number of meshes if directly meshed due to the large number of TSVs. Therefore, it is necessary to simplify the wafer-level simulation model. One-quarter and one-eighth models are usually employed to reduce computation time and degrees of freedom (DOF) according to symmetry of the structure, constraints and loads. However, the number of meshes of the wafer-level finite element model in this paper is still too large to be calculated after applying this method. Therefore, GPD FEM model was adopted as shown in Fig.2. In order to facilitate the description of the birth and death element process, the six-layer bonding model is denoted according to its location. M1-M5 represent the solder between different layers, L1 refers to the part from the bottom layer to M1, L2 refers to the part from M1 to M2, and L3-L6 is similar to L2.

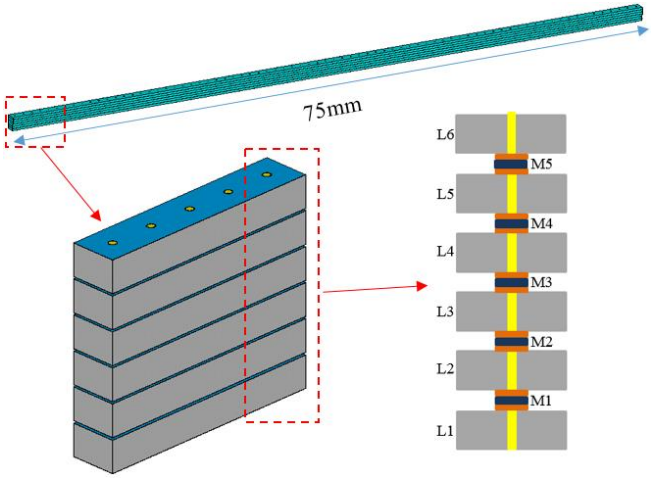

Fig. 2. A finite element model of multilayer stacking

B. *Mesh model and material constants*

The finite element model is meshed by the swept meshing method shown in Fig.3. The number of model elements is 1144320. The material parameters of each part in the finite element model are shown in Table 1. Assuming that Si and SiO_2 are elastic materials, Cu is a temperature-dependent elastic-plastic material. SAC305, Sn63Pb37 and Sn10Pb90 solders are viscoplastic materials shown in Table 2, which are described by the ANAND constitutive equation shown in Table 3.

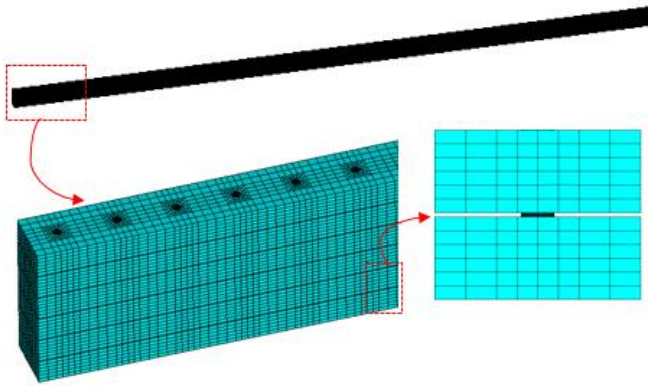

Fig. 3. Meshed GPD model of six-layer stacking

TABLE 1. MATERIAL PROPERTIES

Component materials	E(GPa)	Poisson ratio	CTE (ppm/℃)
Cu	110	0.35	17
Si	129.6(25℃)	0.28	2.81(25℃)
	128.4(150℃)		3.11(150℃)
SiO_2	70	0.16	0.6
SAC305	51	0.4	23.5
Sn63Pb37	56	0.3	20
Sn10Pb90	19	0.28	29

TABLE 2. BI-LINEAR MATERIAL PROPERTIES OF COPPER

Component materials	Yield Strength (MPa)	Tangent Modulus (GPa)
Cu	225	6.666

C. *Stacking process and temperature load*

There are many ways to stack multiple layers of wafers. The stacking process in this paper is a layer-by-layer stacking method. The process flow of multilayer stacking of wafers is shown in Fig.4, in which total six layers of TSV wafer are fabricated with solder bonding processes layer-by-layer.

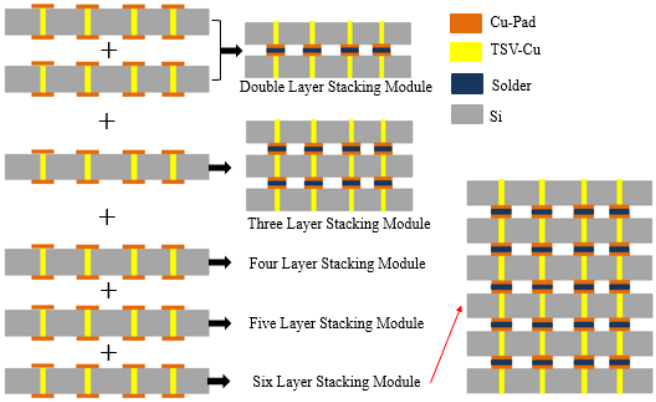

Fig. 4. Schematic of layer-by-layer stacking process

TABLE 3. ANAND MATERIAL CONSTANTS FOR SOLDERS.

Materials	S_0(MPa)	Q/R(1/K)	A(1/sec)	ζ	m	h_0(MPa)	$\hat{s}(MPa)$	n	a
Sn63Pb37	56.33	10830	1.49E7	11	0.303	2640.75	80.415	0.0231	1.34
SAC305	45.9	7460	5.87E6	2	0.0942	9350	58.3	0.015	1.5
Sn10Pb90	15.09	15583	3.25E12	7	0.143	1787	72.73	0.00438	3.73

TABLE 4. THE SETTINGS FOR BIRTH AND DEATH ELEMENT OF SN63PB37

Time(s)	Temperature	birth and death element	Time(s)	Temperature(℃)	birth and death element	Time(s)	Temperature(℃)	birth and death element
0	25	KILL, L3-6 and M1-5	930	25	ALIVE L4	1860	25	ALIVE L6
120	210		1050	210		1980	210	
165	210		1095	210		2025	210	
210	183	ALIVE, M1	1140	183	ALIVE M3	2070	183	ALIVE M5
465	25	ALIVE L3	1395	25	ALIVE L5	2325	25	
585	210		1515	210				
630	210		1560	210				
675	183	ALIVE M2	1605	183	ALIVE M4			

The temperature load for different materials is different due to process differences. Three temperature loading curves and corresponding settings for the birth and death element were given. Fig.5 is the temperature load for three kinds of solder materials. Table 4 shows the temperature values corresponding to each point in the temperature curve. When the solder joint material is Sn63Pb37, the loading temperature curve is as follows. The initial time of the simulation analysis is 0s (25°C), which sets all solder layers (M1-M5) and materials in L3-L6 to the "KILL" state. Set the solder of the M1 layer to "ALIVE" state at 210s (183°C). Then, continue to cool down to 25°C to complete the two-layer wafer simulation analysis at 465s, which is also the start time of the third-layer wafer bonding. The setup of the following temperature loads and the setting for Birth and death element for the third to sixth layers is similar to the second layer. When the solder joints material are SAC305 and Sn10Pb90, the temperature profile is similar to Sn63Pb37.

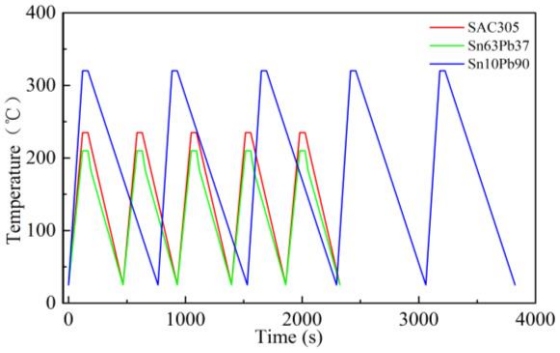

Fig. 5. Temperature load of three kinds of solder materials

III. RESULTS AND DISCUSSIONP

A. Results of Sn63Pb37

The simulation results of Sn63Pb37 solder for six layers model are obtained. Fig. 6 shows the displacement contour in z direction, it is increases gradually with the increase of the number of bonding layers. And the maximum von Mises stress and the maximum equivalent plastic strain on the solder joints are located on the bottommost wafer from Fig. 7. It appears to gradually increase from the middle to the outermost on a single solder joint. The von Mises stress and equivalent plastic strain distribution on the solder joints of the same layer are almost similar, but it gradually increases from the upper to the lower layered solder joint. The reason is that the first layer of solder joints experience more temperature loads throughout the process, so that it is more accumulated plastic deformation.

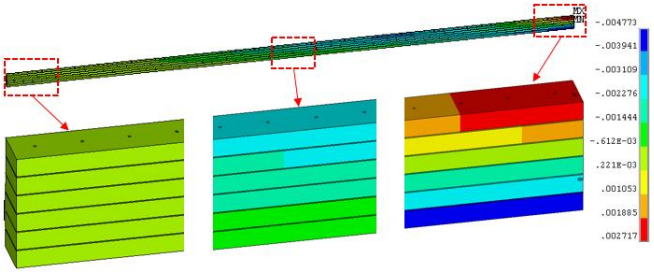

Fig. 6. Displacement contour in z direction

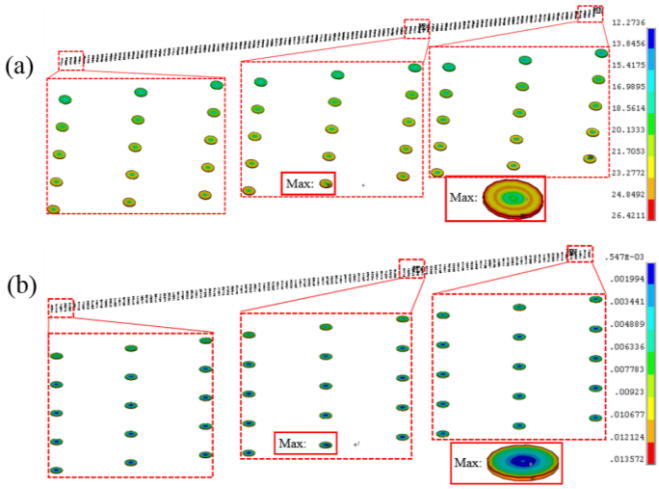

Fig. 7. Stress and strain distribution of the Sn63Pb37 solder joints. (a) von Mises stress (b) equivalent plastic strain

B. Results of three kinds of solder

The simulation results of the six layers wafer bonding model for the three kinds of solders are shown in Fig. 8. It can be seen that the von Mises stress and equivalent plastic strain is volatility rises with bonding process of six layers. The maximum von Mises stress is obtained at Sn63Pb37 solders among the three kind of solders when accomplished six layers bonding, and the Sn10Pb90 is smallest. In which

the maximum von Mises stress is 26.421MPa and the minimum von Mises stress is 16.806Mpa. The maximum equivalent plastic strain is obtained at Sn10Pb90 solders among the three kind of solders when accomplished six layers bonding, and the Sn63Pb37 is smallest. In which the maximum equivalent plastic strain is 0.0424 and the minimum equivalent plastic strain is 0.0136.

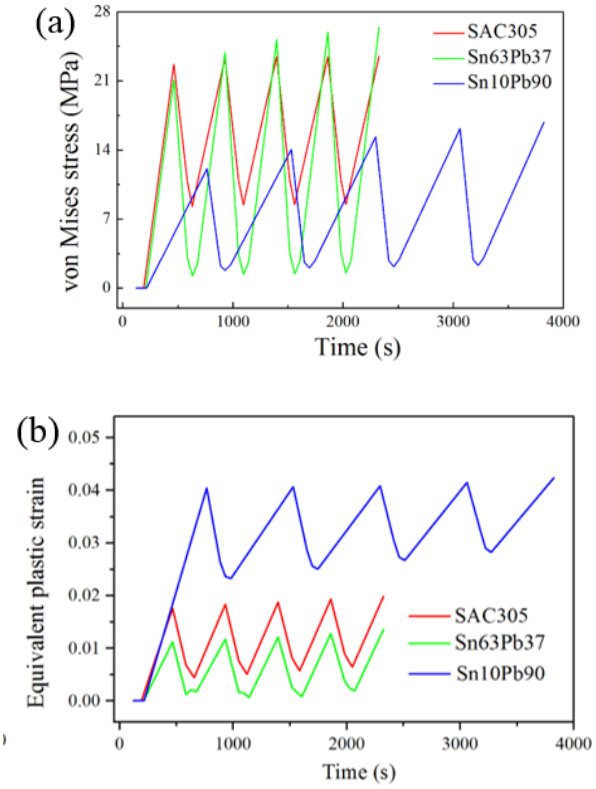

Fig. 8. Analysis results of different material solder joints. (a)von Mises stress (b)equivalent plastic strain

IV. CONCLUTION

According to the investigations presented in this paper, the thermal stress is analyzed for six layered TSV wafer bonded with three kinds of solder materials. The conclusions are drawn as below:

1) The maximum von Mises stress and the maximum equivalent plastic strain on the solder joints are located on the bottommost wafer. The von Mises stress and equivalent plastic strain distribution on the solder joints of the same layer are almost similar, but it gradually increases from the upper to the lower solder joint.

2) The von Mises stress and equivalent plastic strain is volatility rises during the bonding process of six layers.

3) After the numerical analysis for different material solder joints, the maximum von Mises stress is obtained at Sn63Pb37 solders. In contrast, the minimum von Mises stress is obtained at Sn10Pb90 solders. The maximum equivalent plastic strain is obtained at Sn10Pb90 solders, and the minimum equivalent plastic strain is obtained at Sn63Pb37 solders.

REFERENCES

[1] LAU J H. Overview and outlook of three-dimensional integrated circuit packaging, three-dimensional Si integration, and three-dimensional integrated circuit integration. Journal of Electronic Packaging, Vol. 136, 2014.

[2] MOORE G E. No exponential is forever: But “Forever” can be delayed. Proceedings of IEEE International Solid-State Circuits Conference, pp. 20-23. 2003.

[3] K.N. Tu, Reliability challenges in 3D IC packaging technology, Microelectronics Reliability, Vol. 51, pp. 517-523, 2011.

[4] Leila J. Ladani. Numerical analysis of thermo-mechanical reliability of through silicon vias (TSVs) and solder interconnects in 3-dimensional integrated circuits. Microelectronic Engineering, Vol. 87, pp. 208-215, 2010.

[5] Cheng-Ta Ko, Kuan-Neng Chen. Wafer-level bonding/stacking technology for 3D integration. Microelectronics Reliability, Vol. 50, pp. 481-488, 2010.

[6] Z. HAN, Y. WANG, X. YANG. reliability simulation analysis of multilayer chip bonding interface. Transducer and Microsystem Technologies. Vol 3, pp. 50-56, 2020.

[7] Hsin-En Cheng, Rong-Sheng Chen. Interval optimal design of 3-D TSV stacked chips package reliability by using the genetic algorithm method. Microelectronics Reliability, Vol. 54, pp. 2881-2897. 2014.

[8] M. ZHANG, Y. Dai, F, Qin, H. He, J Zheng and H. Zhang. Effect of the accumulated plastic deformation on J-integral for TSV-Cu/SiO2 interface crack under cyclic thermal load. 2020 21st International Conference on Electronic Packaging Technology (ICEPT), pp. 1-4. 2020.

[9] G. Sun, J. Wei, F, Qin, Y. Dai, K. Li and B. Li. Effectiveness Validation on Equivalent Model for Wafer-Level Warpage Prediction. 2021 22nd International Conference on Electronic Packaging Technology (ICEPT), pp. 1-6, 2021.

[10] S. Orain, J.-C. Barbé, X. Federspiel, P. Legallo, H. Jaouen, FEM-based method to determine mechanical stress evolution during process flow in microelectronics, application to stress–voiding[J], Microelectronics Reliability, Vol. 47, pp 295-301, 2007.

[11] Nicole An P, Kohl P A. Modeling Simplification for Thermal Mechanical Analysis of High Density Chip-to-Substrate Connections. Journal of electronic packaging. Vol. 133, 2011.

[12] Kequan Xia, Zhiyuan Zhu, Hongze Zhang. Modeling simplification for thermal mechanical stress analysis of TSV interposer stack[J]. Microelectronics Reliability. pp.46-50, 2019.