Influence of chip layout on temperature distribution of multi-chip press pack IGBT devices

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***Abstract*—Press Pack IGBT(PP IGBT) devices often work under high voltage and high current working conditions, and a multi-chip parallel structure is often used inside the PP IGBT device package. In this structure, the multi-chip layout has an important influence on the temperature distribution of chips. In addition, the chip temperature is closely related to the reliability of the PP IGBT device. Therefore, it is of great significance to study the influence of the internal chip layout of the PP IGBT device on the temperature distribution of the chip. In this paper, the finite element model of the PP IGBT device is established, and the electro-thermal coupling simulation is carried out, and simulate the temperature change of each chip inside the device under the condition of power cycle. First, chip temperature distributions were compared for devices containing a single IGBT chip, four IGBT chips and nine IGBT chips. The junction temperature of the chip is shown as a function of time. Then, the influence of the chip separation distance on the temperature was considered, and the chip temperature distribution was compared under the layouts where each chip and the adjacent chips were separated by 2mm and 4mm, respectively. After analyzing the results of the finite element simulation, it is found that due to the close position of the multiple chips connected in parallel inside the PP IGBT device, thermal coupling effect between chips. This coupling effect affects the temperature distribution of the chip and makes the junction temperature higher. And the more chips and the closer the chip distance, the more obvious the effect of this coupling effect on the chip temperature distribution.**

Keywords—PP IGBT, finite element simulation, temperature coupling, temperature distribution

I. INTRODUCTION

PP IGBT device is a new power semiconductor device, which not only achieves higher power and is easier to connect in series, but also achieves double-sided heat dissipation. Therefore, PP IGBT devices are widely used in the field of power transmission and conversion [1]. As a core component in power equipment, its reliability directly affects the life of the entire equipment. However, PP IGBT devices still face many challenges in practical applications, such as aluminum metallization cracking [2], contact thermal resistance degradation [3] and other reasons leading to failure. Most of the failure causes are thermally related. Thermal issues are a matter of great concern, with approximately 55% of system failures caused by thermal-related issues in power semiconductor devices [4]. Therefore, it is very important to understand the temperature distribution and maximum junction temperature of the IGBT chip to improve reliability.

The junction temperature of the IGBT chip can be obtained through experiments, finite element simulation and RC thermal network model. Y. Zhang et al. [5] directly measured the temperature of the chip near the surface of the emitter side by placing a thermocouple in the trench on the molybdenum side of the emitter. H. Ren et al. [6] removed part of the ceramic shell of a single-chip PP IGBT device, and used an infrared camera to directly obtain the temperature distribution of the internal structure of each layer. To obtain accurate temperature and reduce the influence of reflection, black insulating pigments are coated on the sides of the chip, molybdenum plate, collector Cu and emitter Cu. Both of these experimental methods destroyed the package structure of the PP IGBT device, so they are not suitable for practical situations. A. P. Yu et al. [7] established a finite element model of a PP IGBT device. Through static and transient simulations, the temperature distribution on each chip is obtained. However, they only calculated the temperature of the device for one chip layout, ignoring the effect of chip separation distance on the junction temperature. X. Han et al. [8] established a Cauer thermal network model for PP IGBT devices, which can quickly obtain the junction temperature of the chip under different power losses. But the detailed temperature distribution of each material layer cannot be obtained.

In this paper, the model of a PP IGBT device is established, and the electro-thermal coupling simulation is carried out to simulate the temperature change of each chip inside the device under the condition of power cycling. First, finite element models are established for single-chip devices,

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four-chip devices, and nine-chip devices. Then, the temperature distributions on the surface of IGBT chips under three different chip layouts were compared, and the changes of the maximum junction temperature of each chip during DC power cycling were obtained. Finally, the influence of the chip separation distance on the temperature was considered. The chip temperature distribution was compared under the layouts where each chip and the adjacent chips were separated by 2mm and 4mm, respectively.

II. Preparation before Modeling

A. PP IGBT device

The structure of each component of the PP IGBT device is shown in Fig.1. A device contains multiple identical IGBT submodule groups and FRD submodule groups, which are located between the same collector Cu and the same emitter Cu in a parallel manner. The ceramic shell surrounds the inner chip, there is a PCB board and pedestals at the bottom, and the outer two Cu sheets lead to the gate and the emitter respectively. For a single submodules group, as shown in Fig.2. The collector Mo plate and solder layer are above the IGBT/FRD chip, and the emitter Mo plate and Ag shim plate are below the IGBT/FRD chip. The emitter side of the IGBT chip is sputtered one layer of Al metallization. In addition, there is a gate in the plastic frame of the submodule group to stabilize the structure, and the Mo plates on both sides of the chip relieve the stress generated under working conditions. The various components inside the device are kept electrically connected by external clamping force.

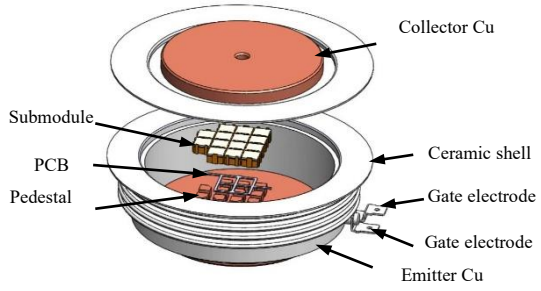


Fig. 1. Internal structure of PP IGBT device.

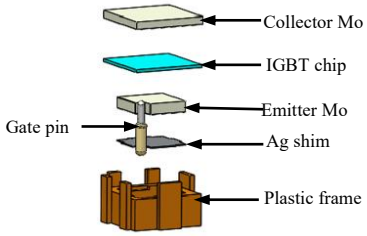


Fig. 2. IGBT chip submodule.

B. DC Power Cycling Experimental Condition

Under the experimental conditions of DC power cycling, the gate is continuously switched on and off by the control of the pulse signal (as shown in Fig.3). In the gate-on state, the load current is introduced from the collector Cu of the PP IGBT device, then passes through each submodule group, and flows out from the emitter Cu to form an electrical path and a thermal path. In the gate-off state, load current cannot be directed into the device. Both sides of the device are dissipated by a constant temperature water-cooled radiator.

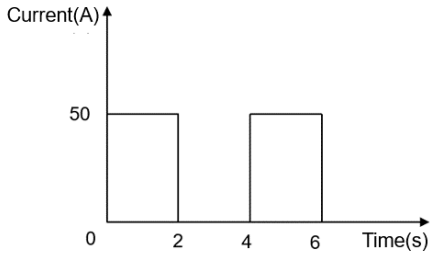


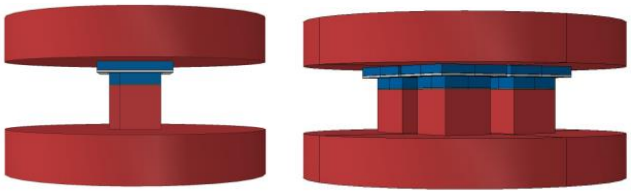
Fig. 3. Current signal under DC power cycling conditions.

III. Finite Element Simulation

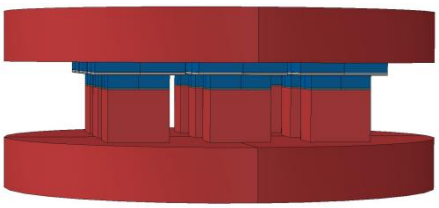
Using ABAQUS software, the model of the PP IGBT device is established, and the electro-thermal coupling simulation is carried out. Finally, the temperature field result of the IGBT chip is obtained.

A. Finite Element Model

The model is simplified without affecting the accuracy of the results. Since the PP IGBT device studied in this paper works under the DC power cycle condition, its FRD sub-chip does not work, so only the IGBT chip submodule is included in the model. And the effect of external ceramic shell, PCB board, plastic frame of submodule group, gate pin on temperature results can be ignored, so there is no need to build their models. The model of the PP IGBT device is established in ABAQUS, as shown in the Fig.4. Table 1 presents the parameters of the different materials included in the device. The established models include single-chip, four-chip, and nine-chip models.



(a) Single chip PP IGBT model. (b) Four chips PP IGBT model.



(c) nine chips PP IGBT model.

Fig. 4. Three PP IGBT models with different numbers of submodules. (a) Single chip PP IGBT model. (b) Four chips PP IGBT model. (c) nine chips PP IGBT model.

TABLE I MATERIAL PROPERTIES

Materials	Eelectrical Conductivity(S/mm)	Thermal conduction (W/m·K)	Specific heat (J/kg·K)	Density (10^{12}kg/ mm^3)
Ag	63.19	429	235	1.05×10^{-8}
Al	37.73	237	900	2.70×10^{-9}
Mo	19.23	138	250	1.02×10^{-8}
Cu	59.52	400	380	8.93×10^{-9}
Si (IGBT)	10.0001299	148	700	2.33×10^{-9}
Solder (SAC305)	9.615	57	230	7.30×10^{-9}

In addition, a model including nine IGBT chips with different separation distances is established, as shown in Fig.5. The relationship between the separation distance of IGBT chips and junction temperature of each chip is studied.

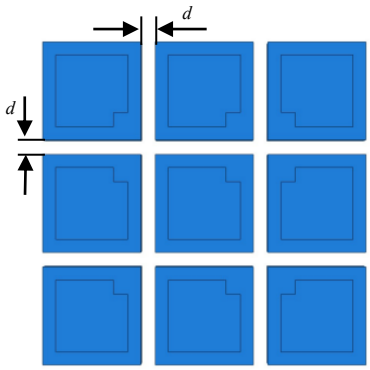


Fig.5. Schematic diagram of the layout of nine IGBT chips.

B. Boundary conditions

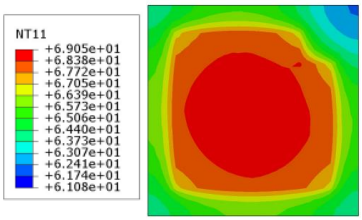
The second part describes the conditions for the DC power cycling, where current is injected at the surface of the collector Cu and then flows out of the emitter Cu. Make sure that the current flowing through each IGBT chip is consistent and rated current. Water cooling heat dissipation is simulated by setting convective heat transfer coefficients on both sides of the model. The heat generated by the chip flows through two heat dissipation paths, one is that the heat is dissipated from the upper side of the chip through the collector Mo plate and the collector Cu. The other is that the heat is dissipated from the underside of the chip through the emitter Mo plate, silver pads, Cu bosses and emitter Cu. We set the ambient temperature to 45°C. There are four surfaces of the material layers in contact with each other. In this paper, the thermal conductivity and electrical conductivity of the contact surfaces are obtained indirectly through experiments.

IV. Results and Discussion

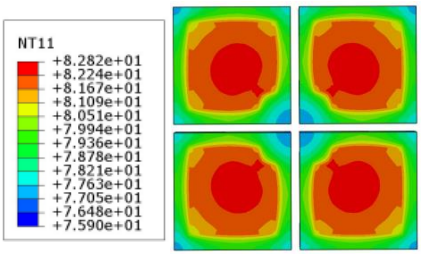
A. Temperature results for chips with different layouts

In the finite element simulation, the average current through the IGBT chip submodules is the same. The temperature distribution of each IGBT chip surface is obtained during DC power cycling. Fig.6 shows the temperature of the surface of the emitter side of the IGBT chip at the 78th s. Among the devices containing a single submodules, four submodules, and nine submodules respectively, the maximum temperatures on the surface of the IGBT chip are 69.05°C, 82.82°C, and 108.6°C, respectively. As shown in the Fig.6(b), for a device containing four submodules, the temperature distributions on the surfaces of the four symmetrically distributed IGBT chips are the same, and the maximum temperatures of the four chips are almost the same. As shown in the Fig.6 (c), in a device containing nine submodules, the highest temperature is in the middle IGBT chip. The temperature distribution of the IGBT chips in the four corners is consistent and the temperature is the lowest. The edge IGBT chips located between the corners have a slightly different temperature distribution. The variation of the maximum junction temperature of the IGBT chip with time for three different chip layouts during DC power cycling is shown in the Fig.7. Among them, the center temperature of the IGBT chip surface of the device containing nine submodules is the highest, the center temperature of the surface of the IGBT chip containing four units is second, and the center temperature of the surface of the IGBT chip containing a single submodule is the lowest.

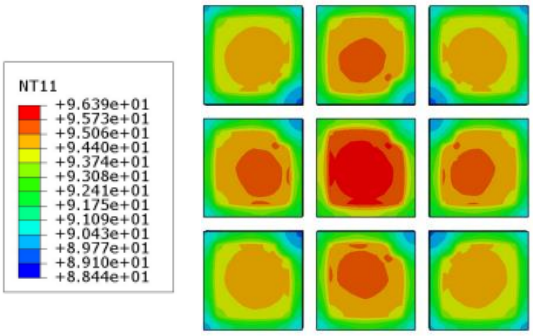
From the finite element temperature field results of three different chip layouts, it can be seen that the chip layout is closely related to the temperature distribution and the highest junction temperature on the chip surface of the PP IGBT device. Due to the small distance between the submodules inside the device, during the DC power cycle, the thermal coupling effect will occur between the submodules, which has a significant impact on the temperature of each IGBT submodule, as shown in the Fig.8. In a device containing four submodules, the four submodules are distributed symmetrically, so the temperature increase due to the coupling effect is approximately the same on the four IGBT chips. In a device containing nine submodules, the submodule in the middle has a mutual thermal coupling effect with the surrounding eight submodules, the edge submodule between the corners has a mutual thermal coupling effect with the surrounding five submodules, and the submodules in the four corners have a mutual thermal coupling effect with the surrounding three submodules. The coupling effect between nine submodules can be extended to devices containing more submodules. Since the coupling effect exceeds a certain distance, the coupling effect can be ignored. Therefore, in a multi-chip PP IGBT device, only these three coupling situations can be considered.



(a) Temperature distribution of a single IGBT chip surface.



(b) Temperature distribution of four IGBT chip surfaces.



(c) Temperature distribution of nine IGBT chip surfaces.

Fig. 6. Temperature distribution of chip surfaces with different layouts. (a) Temperature distribution of a single IGBT chip surface. (b) Temperature distribution of four IGBT chip surfaces. (c) Temperature distribution of nine IGBT chip surfaces.

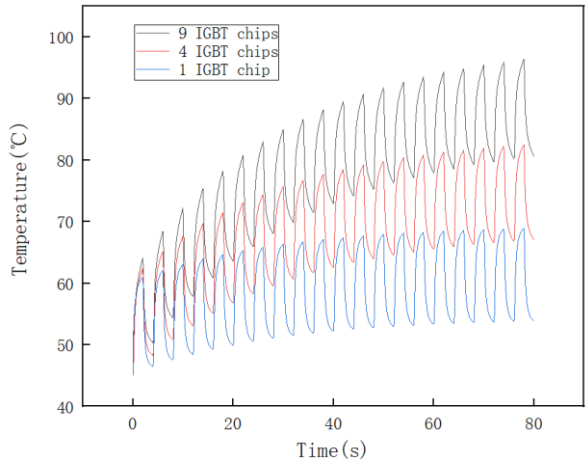


Fig. 7. IGBT chip maximum junction temperature change

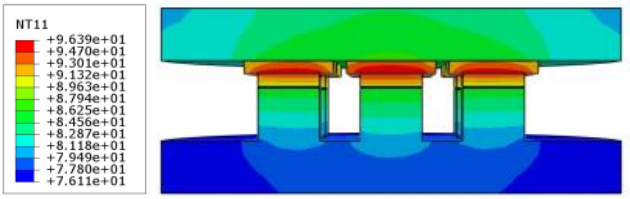


Fig. 8. Cross-section temperature field of PP IGBT device.

B. *Effect of chip separation distance on junction temperature*

When the separation distance between each submodule inside the PP IGBT device changes, the junction temperature of the chip also changes. When the IGBT chip spacing d is 2mm and 4mm respectively, the junction temperature of the center IGBT chip changes with time, as shown in the Fig.9. When the chip separation distance d is 2mm, the maximum junction temperature is higher. As the separation distance increases, the thermal coupling effect between the submodules will decrease accordingly, so the junction temperature will be smaller.

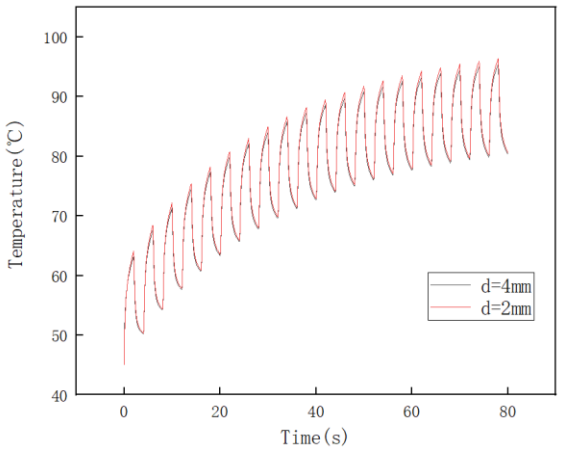


Fig. 9. Junction temperature curve for different chip spacing distances.

V. Conclusion

In this paper, three models of PP IGBT devices with different chip layouts are established, and the electro-thermal coupling simulation is carried out. Finally, the temperature distribution on the surface of the emitter side of each IGBT chip and the change of the junction temperature during DC power cycling are obtained.

In a PP IGBT device containing multiple submodules, there will be significant thermal coupling effects between adjacent submodules. The thermal coupling effect not only affects the temperature distribution of the individual chip surfaces, but also increases the temperature peaks. In a finite element simulation with nine submodules, thermal coupling effects in three cases are shown, and also for devices with more submodules. By comparing the layout of IGBT chips with different separation distancees, the effect of chip separation distance on junction temperature is obtained. When the chip separation distance increases, the thermal coupling effect decreases, and the junction temperature also decreases.

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