

The Effect of the Surface Roughness Characteristics of the Contact Interface on the Thermal Contact Resistance of the PP-IGBT Module

Tong An ¹, Zezheng Li, Yakun Zhang, Fei Qin ¹, Liang Wang, Zhongkang Lin, Xinling Tang, Yanwei Dai ¹, Yanpeng Gong, and Pei Chen ¹

Abstract—In this article, the correlation between the thermal contact resistance and the surface roughness characteristics of the contact interface in the press-pack insulated-gate bipolar transistor (PP-IGBT) modules during power cycling was studied by experimental measurements and finite-element (FE) simulation-based factorial design analysis. Thermal transient test technology was applied to examine the change in the thermal characteristic parameters of the PP-IGBT module. This shows that the increase in the thermal contact resistance of the Al metallization/emitter Mo contact interface occurs more dramatically during power cycling. A 3-D surface profilometer was used to evaluate the surface morphology parameters of the Al metallization/emitter Mo contact interface. The equivalent root-mean-square (RMS) roughness increases during power cycling, and the equivalent asperity slope and the equivalent spacing between asperities increase slightly. Additionally, the surface roughening in the corner area of the chip is more obvious than in other regions. A fractional factorial design analysis based on FE simulations was performed. The results indicate that the thermal contact resistance strongly depends on the main effects of the real contact area and the spacing between the asperities, and the RMS roughness and the asperity slope interaction.

Index Terms—Power cycling, press-pack insulated-gate bipolar transistor (PP-IGBT), surface roughness, thermal contact resistance.

I. INTRODUCTION

WITH HIGH power density, double-side cooling, and short circuit failure, press-pack insulated gate bipolar transistor (PP-IGBT) modules have been widely employed in

high power conversion systems [1]. To maximize the reliability performance, the thermal behavior of PP-IGBT modules is a very significant design consideration, especially in the high power range, since approximately 60% of the cases of failure of power semiconductor devices are thermally induced [2]. Thermal resistance is one of the critical factors that determines the thermal behavior of PP-IGBT modules. In PP-IGBT modules, the IGBT chip is directly connected to two Mo plates and then enclosed by two Cu electrodes. To preserve the thermal contact and electrical contact of these parts, a clamper is applied to provide a clamping force during PP-IGBT module operation. Thus, in contrast to fully bonded interfaces, the total thermal resistance of the PP-IGBT module consists of both thermal resistances of material layers and thermal contact resistances of contact interfaces, which are introduced by the multilayered structure of the PP-IGBT modules. Therefore, knowledge about the thermal contact resistance degradation during PP-IGBT module operation is of great interest.

The value of the thermal contact resistance of the contact interface within the PP-IGBT module depends mainly on the thermal properties of the contact materials, the clamping force, and the surface roughness characteristics of the contact interface [3]. Some researchers dedicate to examining the relationship between the thermal contact resistance and the external clamping force. For a PP-diode module with single chip, Deng *et al.* applied experiments [4] and finite-element (FE) modeling [5] to investigate the effect of the clamping force, thereby indicating that the thermal contact resistance reduces with increasing clamping force. Additionally, Poller *et al.* [6] proposed a method combining the FE analysis results with experimental measurements to incorporate the clamping force sensitivity of thermal contact resistance into the model to describe the electrothermo-mechanical characteristics of a single chip PP-IGBT module. For a multichip PP-IGBT module, the work in [7]–[9] show that an uneven clamping force distribution can cause a partial or even entire loss of contact for the chips in PP housings, which will significantly increase the thermal contact resistance. Furthermore, based on the clamping force, Busca *et al.* [10] calculated the thermal contact resistance of the multichip PP-IGBT module by combining experimental data with analytical calculations.

Another factor that significantly affect the thermal contact resistance is the surface roughness characteristics. The surface morphology of the contact interface, such as the Al

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metallization layer, is not flat but characterized by rugosity [11]. Real mechanical contact between the rough surfaces does not occur on the entire surface but is limited to a portion of the top of the surface asperities. To consider the influence of the surface roughness characteristics, an analytical model has been devoted to calculating the thermal contact resistance [12]. The effect of the surface roughness into an analytical model and employed the model to examine the thermal contact resistances on the Cu/Mo/SiC/Mo/Cu interfaces of a single chip PP-diode module incorporated in [13] and [14]. Deng *et al.* [5] applied FE modeling to estimate the change in thermal contact resistance of the diode chip/collector Mo plate contact interface in a single chip PP-diode module, thereby indicating that a surface roughness decrease leads to a lower thermal contact resistance. Although some related studies have considered the effect of the surface morphology on the thermal contact resistance, relatively few research efforts have been devoted to measure the evolution of the contact interface roughness within PP-IGBT module subjected to power cycling and the dependency of the thermal contact resistance on the surface morphology parameters of the contact interface.

The aim of this article is to study the correlation between the thermal contact resistance degradation and the evolution of the contact surface morphology in the PP-IGBT module subjected to the power cycling test. The thermal contact resistance of the Al metallization/emitter Mo interface was examined at different power cycling aging times. The surface morphology parameters of the Al metallization/emitter Mo interface were measured and employed to characterize the surface roughness evolution of the contact interface. Factorial design analysis based on qualitative FE modeling with the technique of submodeling was performed to investigate the influences of the surface roughness characteristics of contact interface on its thermal contact resistance. Based on the factorial analysis, the main effects of the surface morphology parameters on the thermal contact resistance degradation were determined.

II. EXPERIMENTAL PROCEDURES

A. Tested PP-IGBT Module

The typical electrical ratings of the considered PP-IGBT module are 3300 V/50 A. the tested device was a single chip 3300 V/50 A PP-IGBT module. The PP-IGBT module consists of a collector Cu plate, collector Mo plate, Sn3.0Ag0.5Cu solder layer, IGBT chip, and Al metallization layer, which are deposited onto the Si die, emitter Mo plate, Ag shim plate, and emitter Cu plate, as shown in Fig. 1.

Four IGBT modules were applied here, module A⁰, module B¹⁰⁰, module C²⁵⁰, module D⁴⁰⁰, and the superscript in the sample labels represent the number of cycles the module has experienced.

B. Power Cycling Test

As shown in Fig. 2, the power cycling test bench consists of a power supply system, a control system, a drive system, a data acquisition system, and a water-cooling system. The clammer

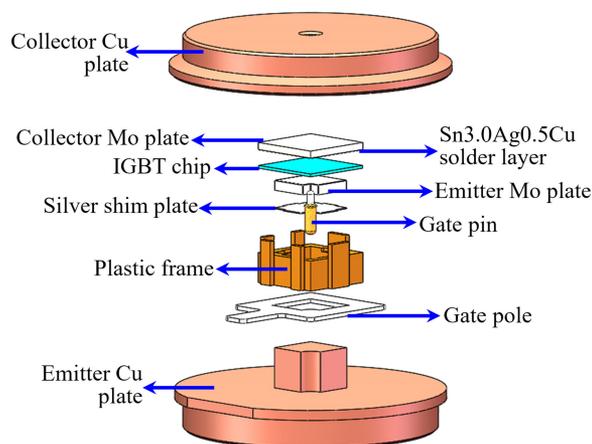


Fig. 1. Schematic of the PP-IGBT module.

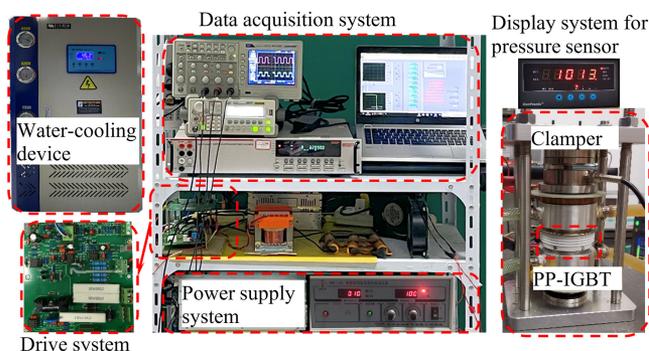


Fig. 2. Prototype of the test setup.

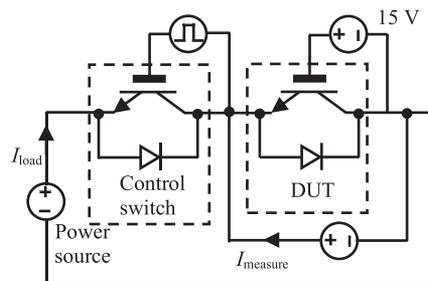


Fig. 3. Circuit of the dc power cycling test.

was employed to maintain the needed clamping force and provided double-sided water cooling. According to the mounting instruction that a pressure of approximately 1.2 kN/cm² is ideal for PP IGBTs [15], [16]. Therefore, a clamping force of 1.01 kN was applied to the PP-IGBT module according to its clamped area.

Fig. 3 presents the circuit diagram of the dc power cycling test. A constant dc voltage (e.g., 15 V) was employed to the gate to keep the device under test on during the test. When the control switch was on, a current I_{load} was injected into the PP-IGBT module. As a result, the junction temperature T_j of the PP-IGBT module started to increase due to its conduction power loss. Then, the applied load current was disconnected by turning off

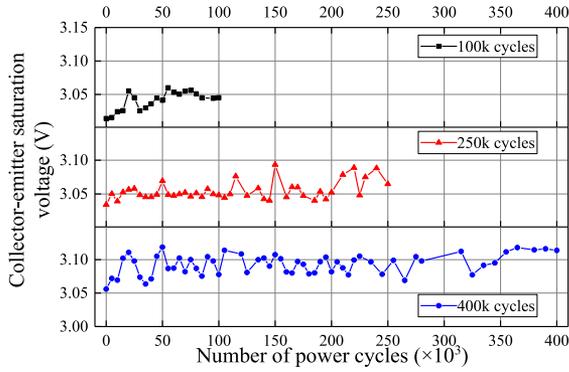


Fig. 4. Evolution of the V_{CEsat} over aging time.

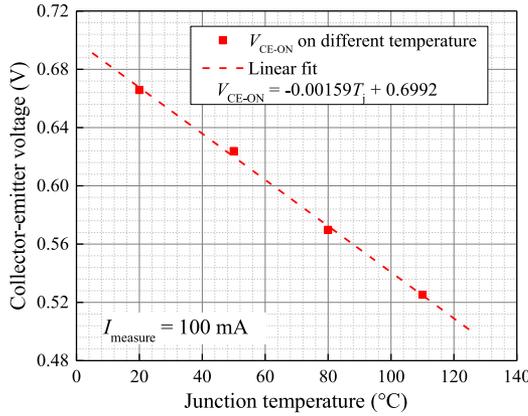


Fig. 5. Calibration curve of V_{CE-ON} and T_j with a constant measurement current of 100 mA for the PP-IGBT module.

the control switch, and the temperature of the PP-IGBT module was decreased by the double-side cooling system.

All the power cycling tests discussed in this article were conducted with a constant t_{on}/t_{off} control strategy without compensation for degradation, and $t_{on} = 2$ s and $t_{off} = 2$ s were set, which means that the total cycling period was 4 s. The load current for the tests was set to 50 A, and the water-cooling system had a constant water temperature of 45 °C. Under these test conditions, the initial junction temperature swing was approximately 54.21–62.1 °C. Four PP-IGBT modules were tested for 0, 100, 250, and 400 k power cycles, respectively.

During the power cycling tests, the collector-emitter saturation voltages V_{CEsat} of the tested PP-IGBT modules were measured under the load current at room temperature every 5000 cycles. As shown in Fig. 4, with increasing number of cycles, V_{CEsat} is almost constant. The maximum increases of V_{CEsat} for the module B¹⁰⁰, module C²⁵⁰, module D⁴⁰⁰ are approximately 1.53%, 1.96% and 2.05%, respectively, indicating the devices were still functional after tests, and no obvious failure occurred.

To estimate the T_j of the under tested modules during power cycling tests, a preliminary calibration was conducted to obtain the dependence of T_j on the ON-state collector-emitter voltage V_{CE-ON} for the PP-IGBT module with a constant current of 100 mA [17], [18]. Fig. 5 shows the characterization curve of V_{CE-ON} and T_j , and the temperature sensitivity (K factors) is

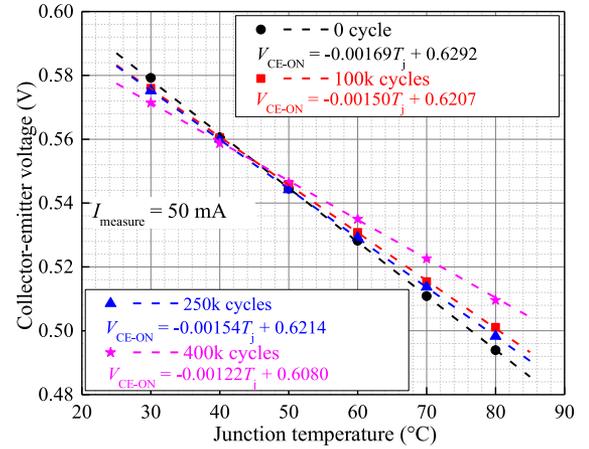


Fig. 6. Calibration curves of V_{CE-ON} and T_j with a constant measurement current of 50 mA for the PP-IGBT modules after power cycling tests.

approximately -1.59 mV/°C. During the power cycling test, the V_{CE-ON} of the PP-IGBT module was measured with a constant measurement current, $I_{measure}$, of 100 mA, when the load current was disconnected.

C. Experimental Determination of the Thermal Contact Resistance Within the PP-IGBT Module

For the estimation of the T_j in the transient thermal impedance Z_{th} curve measurement, a preliminary calibration was performed to obtain the dependence of T_j on V_{CE-ON} for the PP-IGBT modules after power cycling tests with a constant current of 50 mA [17], [18]. As shown in Fig. 6, the K factors are approximately -1.69 mV/°C for Module A⁰, -1.50 mV/°C for module B¹⁰⁰, -1.54 mV/°C for module C²⁵⁰, and -1.22 mV/°C for module D⁴⁰⁰, indicating that the K factor decreases as the number of power cycles increases.

Then, the transient thermal impedance Z_{th} curves of the PP-IGBT modules before and after power cycling were measured using a thermal transient tester (T3Ster). A heating current of 50 A was injected into the PP-IGBT module by turning ON the control switch until it reached thermal equilibrium. Afterward, the control switch was turned OFF, and V_{CE-ON} was measured during the cooling duration. The PP-IGBT module was under emitter-side cooling, and the collector side was adiabatic. T_j can be calculated from the recorded V_{CE-ON} and K factors. Therefore, the transient thermal impedance $Z_{th, cooling}(t)$ that describes the cooling behavior of the PP-IGBT module can be estimated by

$$Z_{th, cooling}(t) = \frac{T_j(t) - T_j(t=0)}{P} \quad (1)$$

where P is the power dissipation measured shortly before the moment when the power is turned OFF.

As the tested PP-IGBT modules are under emitter-side cooling, the preferred heat flow path is from the IGBT chip, Al metallization layer, emitter Mo plate, silver shim plate, emitter Cu plate and finally into the heat sink region, and the heat conduction process can be modeled by an equivalent resistance capacitance (RC) thermal network, as shown in Fig. 7. In the

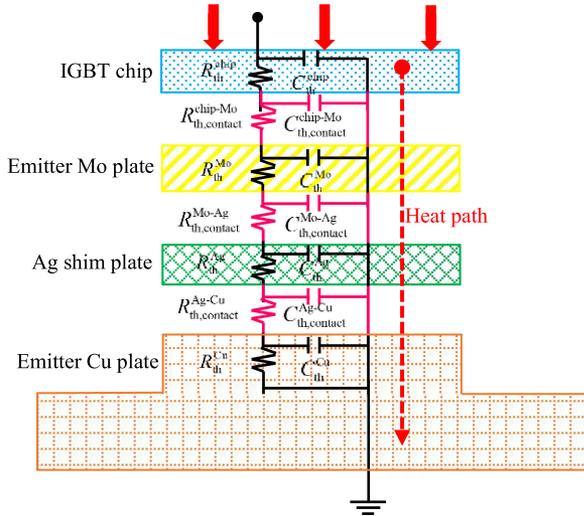


Fig. 7. RC thermal network of PP-IGBT module.

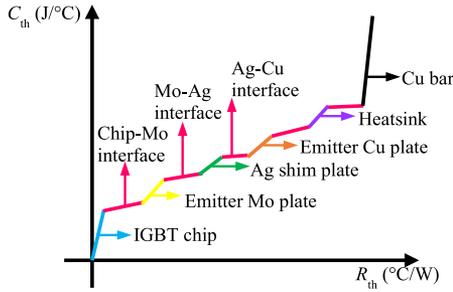


Fig. 8. Schematic diagram of cumulative structure function of PP-IGBT module.

RC thermal network, an RC unit is applied to represent the heat conduction characteristic of each material layer or each contact interface, which includes an equivalent thermal capacitance C_{th} and an equivalent thermal resistance R_{th} .

Finally, to estimate the thermal resistance of the material layers R_{th} and the thermal contact resistance $R_{th,contact}$ of contact interfaces, the $Z_{th,cooling}(t)$ curve was converted to the corresponding cumulative and differential structure function [4], [19]–[21]. The cumulative structure function is the cumulative thermal capacitance $C_{th\Sigma}$ as a function of the cumulative thermal resistance $R_{th\Sigma}$ along the heat-flow path from the junction to the heatsink. A change in the slope in the cumulative structure function represents that the heat flows into a different material layer/surface, and thus, it allows us to identify the R_{th} and the $R_{th,contact}$ [19], [21], as illustrated in Fig. 8. The differential structure function is the derivative of the cumulative structure function. A local peak in the differential structure function represents a different material layer/surface in the heat flow path.

D. Analysis of the Al Metallization/Emitter Mo Interface Roughness

The tested PP-IGBT module was opened for the measurement of the surface roughness characteristics. The surface morphology parameters of the Al metallization/emitter Mo

interface before and after power cycling were quantitatively measured using a 3-D surface profilometer. Two test points on the tested contact surface were chosen for each sample, i.e., T1-the central area, and T2-the area at the corner of the chip [see Fig. 9(a)]. The 3-D surface topography images of each test position were acquired in a $30\ \mu\text{m} \times 30\ \mu\text{m}$ size area. Four profile paths, two along the x direction and two along the y direction, across the tested surface were selected, and the height profiles were extracted [see Fig. 9(b) and (c)]. The geometric characteristics of the height profile can be described by estimating standardized statistical parameters, namely, the root mean square (RMS) roughness σ the RMS asperity slope m and the mean spacing between asperities λ which are given by

$$\sigma = \sqrt{\frac{1}{N} \sum_{i=1}^N z_i^2} \quad (2)$$

$$m = \sqrt{\frac{1}{N} \sum_{i=1}^N \left[\frac{dz_i(x_i, \text{or } y_i)}{d(x_i, \text{or } y_i)} \right]^2} \quad (3)$$

$$\lambda = \frac{1}{N} \sum_{i=1}^N \lambda_i \quad (4)$$

where z_i is the distance between the mean plane and the points on the height profile, N is the number of z_i , and λ_i is the spacing between asperities, as illustrated in Fig. 9(d). The surface morphology parameters of both Al metallization and emitter Mo plate were measured. It has been assumed that the contact between two rough surfaces is simplified to the contact between a rough surface and a perfectly smooth surface, which has equivalent surface characteristics [22]. Thus, the equivalent RMS roughness σ_{eq} the equivalent RMS asperity slope m_{eq} and the equivalent mean spacing between asperities λ_{eq} used to characterize the Al metallization/emitter Mo interface are defined as [23]

$$\sigma_{eq} = \sqrt{\sigma_{Al}^2 + \sigma_{Mo}^2} \quad (5)$$

$$m_{eq} = \sqrt{m_{Al}^2 + m_{Mo}^2} \quad (6)$$

$$\lambda_{eq} = \sqrt{\lambda_{Al}^2 + \lambda_{Mo}^2} \quad (7)$$

where σ_{Al} and σ_{Mo} are the RMS roughness, m_{Al} and m_{Mo} are the RMS asperity slope, and λ_{Al} and λ_{Mo} are the mean spacing between asperities of the Al metallization and the Mo plate, respectively.

III. MODELING PROCESS

A. Submodeling of PP-IGBT Module

To further understand the dependency of the thermal contact resistance on the surface roughness characteristics of the Al metallization/emitter Mo interface, a submodeling technique was applied, as depicted in Fig. 10. In the global model, the 3-D FE model of the PP-IGBT module was established according to the test sample, in which the collector Cu plate, collector Mo plate, Sn3.0Ag0.5Cu solder layer, IGBT chip, Al metallization layer,

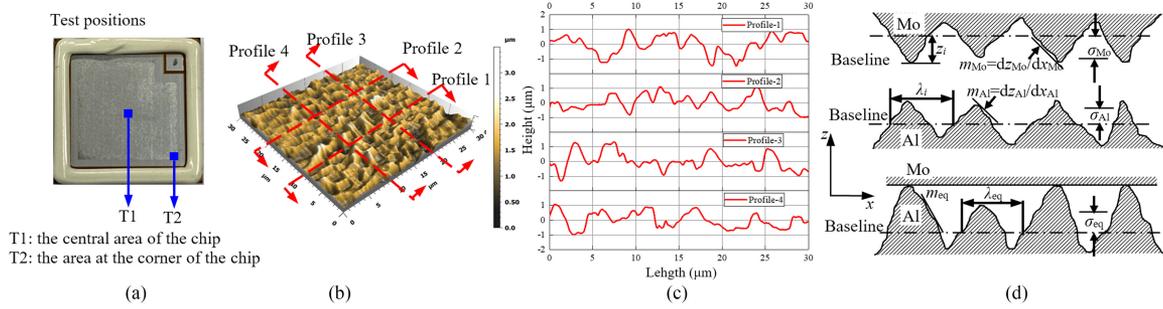


Fig. 9. Definition of the surface roughness parameters. (a) Sample of the IGBT chip. (b) 3-D surface-topography images. (c) Extracted height profiles. (d) Definition of the profile geometry characteristics parameters.

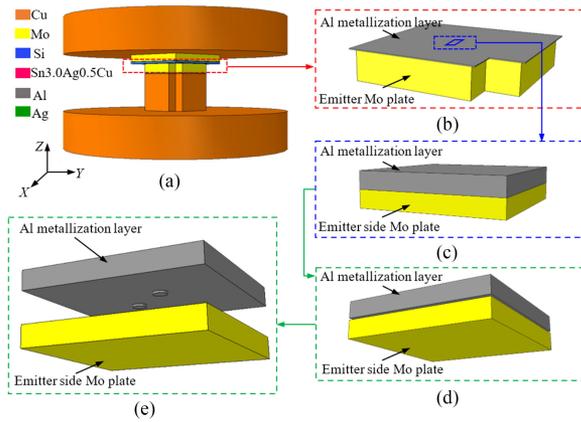


Fig. 10. FE model of PP-IGBT module. (a) Global model. (b) First-level submodel. (c) Second-level submodel. (d) Third-level submodel. (e) Exploded view of third-level submodel.

emitter Mo plate, silver shim plate, and emitter Cu plate were considered, as depicted in Fig. 10(a). The geometric dimensions of the global model were the same as that of the test sample, as given in Table I.

To facilitate the boundary condition transfer from the global model to the submodel, three levels of the submodel have been constructed. The first-level submodel consists of an Al metallization layer and an emitter Mo plate, which is exactly the same size as that in the global model [see Fig. 10(b)]. Then, the cut boundaries of the second-level submodel were defined along the perimeter sides of a cuboid with dimensions of $200 \mu\text{m} \times 200 \mu\text{m} \times 50 \mu\text{m}$ for the Al metallization layer and a cuboid with dimensions of $200 \mu\text{m} \times 200 \mu\text{m} \times 50 \mu\text{m}$ for the emitter Mo plate from the first-level submodel [see Fig. 10(c)]. Finally, in the third-level submodel, the interface roughness was considered, where cylinders or cones were created on the Al metallization surface [see Fig. 10(e)]. Here, only the Al metallization layer has a rough surface, and the emitter Mo plate has a perfectly smooth surface. The linear elastic material properties were used in the FE analysis and are given in Table II.

B. Fully Coupled Thermal-Electrical-Structural Analysis

During the modeling of the PP-IGBT module operation, the electrical, thermal, and mechanical solutions strongly affect

TABLE I
DIMENSIONS OF THE FE MODEL

Components	Dimension (mm)	Schematic
Collector Cu plate	$r = 24, h = 8$	
Collector Mo plate	$a = 9.4, h = 2$	
IGBT chip	$a = 13.6, h = 0.37$	
Al metallization layer	$a = 13.6, b = 11.6, c = 2, h = 0.05$	
Ag shim plate	$a = 9.4, b = 7.4, c = 2, h = 0.2$	
Emitter Mo plate	$a = 9.4, b = 7.4, c = 2, h = 2$	
Emitter Cu plate	$r = 24, a = 9.4, b = 9.4, c = 2, d = 48, h_1 = 8, h_2 = 8;$	

TABLE II
MATERIAL PROPERTIES APPLIED IN THE ELECTROTHERMAL FE ANALYSIS

Materials	Young's modulus (GPa)	Poisson's ratio	Coefficients of thermal expansion (ppm/°C)	Thermal conduction (W/m·K)	Electrical conductivity (1/mΩ·mm)	Density (kg/m³)	Specific heat (J/kg·K)
Si ^[24]	113	0.29	3.0	150	0.01	2330	700
Cu ^[24]	103	0.3	17.0	400	58.82	8920	380
Al ^[24]	70	0.33	24.5	235	37.73	2700	900
SnAgCu ^[25, 26]	37.4	0.34	22.9	30	5.88	7440	192
Mo ^[27]	312	0.3	5.1	138	19.23	10200	250
Ag ^[28]	76	0.37	19.6	429	68.03	10500	235

each other. The Joule heat arises from the electrical current flowing through material layers within the PP-IGBT module. In addition, thermal expansion of the material layers occurs as the temperature changes, and at the contact interfaces, constrained thermal expansion induces significant pressure. Additionally, the heat and electricity conducted between contact interfaces depend strongly on the pressure transmitted across the surfaces. To simultaneously obtain solutions for the displacement, temperature, and electrical fields, we performed a fully coupled thermal–electrical–structural analysis.

The eight-node coupled thermal-electrical-structural elements, type Q3D8 in ABAQUS, were employed to mesh the whole model. There were 72 206 elements and 81 459 nodes in the global model, 41 961 elements and 47 680 nodes in the first-level submodel, 25 000 elements and 28 611 nodes in the second-level submodel, and approximately 68 878 elements and 81 907 nodes in the third-level submodel.

The behavior of the global model was analyzed first. A clamping force of 1.01 kN was applied to the top surface of the collector Cu plate. All the nodes at the bottom surface of the emitter Cu plate were constrained for the degree of freedom in the Z-direction, and one node at bottom surface was constrained for all degrees of freedom to limit rigid body displacement. After the first step of the calculation, the force loading was deactivated, and the displacement between the top and bottom surfaces of the global model was constrained to represent the boundary conditions provided by the clammer during the power cycling tests. An electrical current of 50 A was injected at the top surface of the collector Cu plate. The current flowed through the conductor layers of the PP-IGBT module and finally into the zero-potential region at the bottom surface of the model. A temperature boundary condition of 45 °C was used on the top and bottom surfaces of the model to simulate the effect of the double-sided cooling system. Both the ambient temperature and the stress-free temperature of the model were set to 23 °C.

Then, the displacement and temperature results calculated on the cut boundary of the global model were interpolated and employed as boundary conditions for the first-level submodel, and the simulation of the first-level submodel was conducted with the interpolated boundary conditions. For the second-level and third-level submodels, the same analysis procedures were performed. The heat flux q and difference in temperature between the surfaces ΔT were obtained by FE simulations. Finally, the thermal contact resistance $R_{th,contact}$ of the contacting Al metallization/emitter Mo interface in the third-level submodel can be estimated by the following formula:

$$R_{th,contact} = \frac{\Delta T}{qA} \quad (8)$$

where A is the contact area.

IV. RESULTS AND DISCUSSION

A. Thermal Resistance Evolution of the PP-IGBT Module

As shown in Fig. 11, the cumulative and differential structure functions of the PP-IGBT modules aged for different numbers of power cycles were obtained. After 400 k cycles, the curve

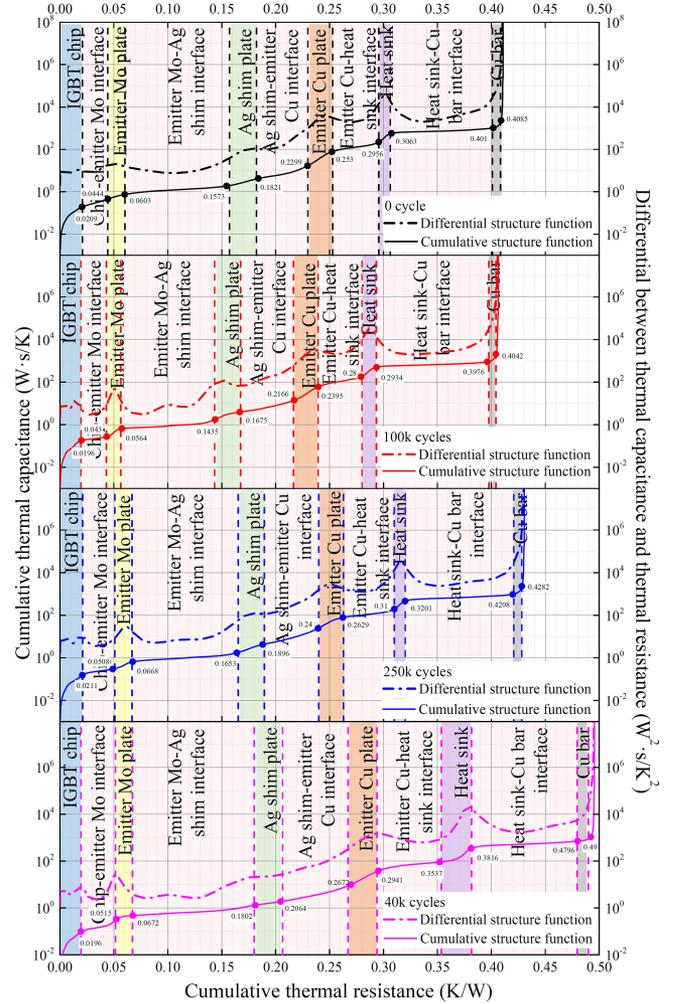


Fig. 11. Cumulative and differential structure functions of the PP-IGBT module.

shifts to the right, thereby indicating that as the number of cycles increases the total thermal resistance of the PP-IGBT module increases.

To estimate the value of thermal resistance of each material layer R_{th} the cumulative structure function curve was split by the inflection points where the slope changes, as this change in the slope represents a transition in the material layer, and thus the R_{th} is the difference in the abscissa values between the two inflection points. The thermal resistances of each material layer aged for different numbers of power cycles are given in Table III. Before aging, the thermal resistances of the IGBT chip, emitter Mo plate, Ag shim plate, and emitter Cu plate were 0.02090, 0.0158, 0.0247, and 0.0231 K/W, respectively. After 400 k cycles, there is an insignificant enhancement in the thermal resistances for IGBT chip, emitter Mo plate and Ag shim plate, and the maximum percent of change in the thermal resistance is approximately -6.316% . The thermal resistance of emitter Cu plate did not change significantly after 250 k cycles, but it increased significantly from 250 k cycles to 400 k cycles.

The thermal contact resistances of contact interfaces $R_{th,contact}$ within PP-IGBT module can also be determined from

TABLE III
MEASUREMENT RESULTS OF THERMAL RESISTANCE OF MATERIAL LAYERS
WITHIN PP-IGBT MODULE

Material layer	Thermal resistance (K/W)				
	0 cycles	100k cycles	250k cycles	400k cycles	Increase rate
IGBT chip	0.0209	0.0196	0.0212	0.0196	-6.316%
Emitter Mo plate	0.0158	0.0135	0.0160	0.0157	-0.569%
Ag shim plate	0.0247	0.0240	0.0243	0.0261	5.659%
Emitter Cu plate	0.0231	0.0229	0.0228	0.0269	16.508%

TABLE IV
MEASUREMENT RESULTS OF THERMAL CONTACT RESISTANCE OF CONTACTING
INTERFACES WITHIN PP-IGBT MODULE

Material layer	Thermal contact resistance (K/W)				
	0 cycles	100k cycles	250k cycles	400k cycles	Increase rate
Al metallization/Emitter Mo plate	0.0235	0.0234	0.0297	0.0319	35.672%
Emitter Mo plate/Ag shim plate	0.0971	0.0871	0.0985	0.1130	16.411%
Ag shim plate/Emitter Cu plate	0.0478	0.0491	0.0505	0.0608	27.111%

the cumulative structure function curve. At the contact interfaces, the low thermal conductivities of interstitial gases and the small real contact area led to a relatively high thermal resistance, thereby showing a relatively low slope on the cumulative structure function curve. As given in Table IV, initially, the thermal contact resistances of the Al metallization/emitter Mo interface, emitter Mo/Ag shim interface, and Ag shim plate/emitter Cu are 0.0235, 0.0971, and 0.0478, respectively. During power cycling, a great raise in the thermal contact resistance can be seen. Especially at the Al metallization/emitter Mo interface, the thermal contact resistance increases to 0.0319 K/W after 400 k power cycles, which is a 35.672% increase.

It clearly indicates that the thermal resistance within the PP-IGBT module increases slightly, while the increase in the thermal contact resistance occurs more dramatically during power cycling. Additionally, the Al metallization/emitter Mo interface experiences a relatively high enhancement in the thermal contact resistance compared to that on other interfaces, and thus, the following discussion will focus on the evolution of the interface roughness of the Al metallization/emitter Mo contact interface and its effect on the thermal contact resistance.

B. Surface Roughness Characteristics of the Al Metallization/Emitter Mo Contact Interface

Table V gives the 3-D surface topography images and the height profiles obtained from the corner area of the Al metallization and emitter Mo plate aged for different numbers of power cycles. To further estimate the change of the surface morphology, Table VI gives the RMS roughness σ_{Al} and σ_{Mo} the RMS asperity slopes m_{Al} and m_{Mo} the mean spacing between asperities λ_{Al} and λ_{Mo} of two different scanning areas of the Al metallization and the emitter Mo plate, and the equivalent

surface roughness parameters of the Al metallization/emitter Mo contact interface σ_{eq} , m_{eq} , and λ_{eq} for different numbers of cycles.

For the surface of the Al metallization layer, initially, the RMS roughness σ_{Al} of the central (T1) and corner (T2) test positions are approximately the same. Then, the σ_{Al} increases during the power cycling process at both test positions. However, the surface roughening is not consistent across the entire surface. After 400 k cycles σ_{Al} raises from 0.2704 to 0.6861 μm at the corner test position (T2), indicating the σ_{Al} after power cycling is 2.5 times that before power cycling. It shows that the surface morphology of the Al metallization layer experiences a comparatively great change in the corner region; at the same time, in contrast, σ_{Al} increases from 0.2762 to 0.3289 μm in the central region (T1), which is only a 19.08% increase, thereby showing a relatively small change of the surface morphology at this test position. This shows that the RMS roughness of the Al metallization continually increases under power cycling condition, and the surface roughening in the corner region is more obvious. In addition, with the increase in the number of cycles, the RMS asperity slopes and the mean spacing between asperities of the Al metallization increase in both test regions.

The surface roughening, or reconstruction, of the Al metallization layer in the typical wire-bonded IGBT module has been widely reported [29]–[31]. The periodic thermal stresses induced by the temperature variations and the coefficient of thermal expansion (CTE) mismatch between Si (3 ppm/K) and Al (24.5 ppm/K) are the major causes of this plastic deformation of the Al metallization layer. However, for a single chip PP-IGBT module, the maximum junction temperature reached during power cycling is approximately 62.14 °C, which is clearly lower than that in wire-bonded IGBT modules, which normally reach 110 °C. Therefore, the low junction temperature makes the thermal-induced stresses of the Al metallization layer lower than the elastic limit, which will not induce severe plastic deformation. Thus, the changes of the surface morphology in the Al metallization layer of the PP-IGBT module cannot be totally attributed to the thermal-induced stress.

In addition to the thermal stress, temperature variations and mismatches in the CTE of Al (24.5 ppm/K) and Mo (5.1 ppm/K) can also induce fretting wear [11], [32]. During power cycling, local relative sliding occurs on the Al metallization/emitter Mo plate contact interface, thereby activating fretting damage. The fretting wear can be used to explain the higher roughness at the corner region of the Al metallization layer. The expansion is relatively serious in the corner area, and thus, the Al metallization/emitter Mo plate contact interface in the corner undergoes a relatively severe fretting wear compared to that of other areas, thereby inducing a more obvious roughness change at the corner test position.

For the surface of emitter Mo plate, the RMS roughness σ_{Mo} in both test regions has a relatively small change during power cycling compared with that observed in the Al metallization layer. In the central region (T1) σ_{Mo} increases by 9.77% from 0.4166 to 0.4573 μm , and in the corner region (T2), σ_{Mo} increases by 14.89% from 0.4198 to 0.4823 μm . The change in

TABLE V
3-D SURFACE TOPOGRAPHY IMAGES AND PROFILES OF THE AL METALLIZATION AND EMITTER MO PLATE

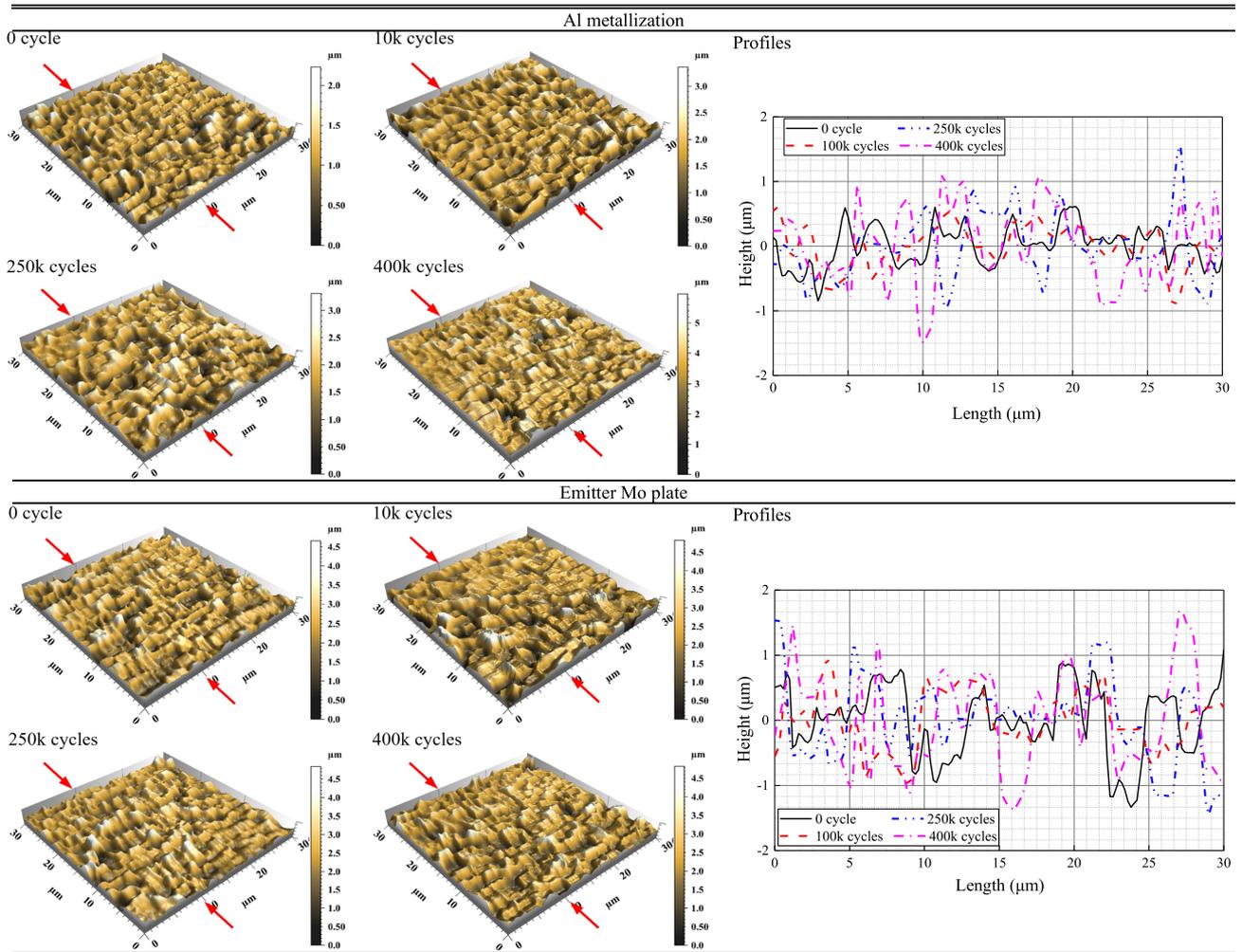


TABLE VI
MEASUREMENT RESULTS OF THE SURFACE ROUGHNESS PARAMETERS OF THE AL METALLIZATION/EMITTER MO PLATE INTERFACE

Surfaces	Cycles ($\times 10^3$)	The central area (T1)			The corner area (T2)		
		RMS roughness σ (μm)	Asperity slope m/angle (degree)	Mean spacing between asperities λ (μm)	RMS roughness σ (μm)	Asperity slope m/angle (degree)	Mean spacing between asperities λ (μm)
Al metallization layer	0	0.2762	0.6249/32.002	3.2929	0.2704	0.6296/32.197	3.0976
	100	0.2818	0.6555/33.243	3.2750	0.3549	0.7632/37.350	3.5175
	250	0.3097	0.6593/33.396	4.1050	0.5763	0.8547/40.520	4.3400
	400	0.3289	0.7170/35.631	3.8869	0.6861	1.0272/45.768	4.0452
	Increase rate	19.080%	14.738%/11.340%	18.039%	153.735%	63.151%/42.150%	30.591%
Emitter Mo plate	0	0.4166	0.9361/43.109	3.3721	0.4198	0.9131/42.400	3.6532
	100	0.4034	0.8299/39.688	3.4851	0.3723	0.9211/42.648	3.57875
	250	0.4079	0.8735/41.137	3.2702	0.4257	0.9557/43.703	3.6125
	400	0.4573	0.9743/44.253	3.3916	0.4823	0.9464/43.422	4.4075
	Increase rate	9.770%	4.081%/2.654%	0.578%	14.888%	3.647%/2.410%	20.648%
Al/Mo interface	0	0.4998	1.1255/48.380	4.7132	0.4993	1.1091/47.962	4.7897
	100	0.4921	1.0576/46.604	4.7824	0.5144	1.1962/50.105	5.0180
	250	0.5121	1.0943/47.580	5.2484	0.7165	1.2821/52.048	5.6467
	400	0.5633	1.2097/50.421	5.1586	0.8387	1.3967/54.398	5.9824
	Increase rate	12.694%	7.479%/5.822%	9.450%	67.951%	25.930%/18.501%	24.903%

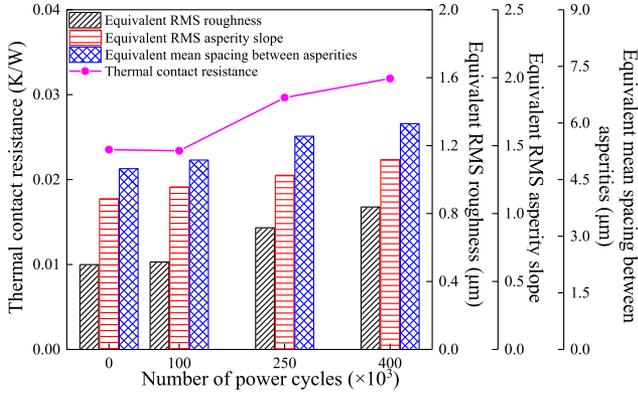


Fig. 12. Relationship between the thermal contact resistance and the morphology parameters of the Al metallization/Mo contact interface.

the RMS asperity slope and the mean spacing between asperities of the emitter Mo plate surface is small.

Then, the equivalent RMS roughness σ_{eq} the equivalent RMS asperity slopes m_{eq} and the equivalent mean spacing between asperities λ_{eq} for the contacting Al metallization/Mo interface were calculated based on (5)–(7) and are given in Table VI. After 400 k power cycles, the σ_{eq} at the corner test position (T2) increases from 0.4993 to 0.8387 μm , which is a 67.95% increase, and at the central test position (T1), it increases by 12.69% to 0.5633 μm . In addition, the m_{eq} and the λ_{eq} change slightly. This surface roughness change will definitely affect the thermal contact resistance. In one analytical model for the thermal contact resistance $R_{th, contact}$ is given by [12], [33]

$$R_{th,contact} = \frac{1}{A \cdot h_{th,contact}} \quad (9)$$

where A is the nominal contact area and $h_{th, contact}$ represents the thermal contact conductance, which is defined as

$$h_{th,contact} = \frac{1.25m_{ab}k_s}{\sigma_{eq}} \left(\frac{P}{H_c} \right)^{0.95} \quad (10)$$

where σ_{eq} , m_{ab} , k_s , P , and H_c refer to equivalent RMS surface roughness, equivalent mean absolute surface slope, harmonic mean thermal conductivity, contact pressure and contact microhardness, respectively. Based on the model, the increasing surface roughness and decreasing asperity slope will raise the thermal contact resistance.

C. Effect of the Contact Interface Morphology on the Thermal Contact Resistance

Fig. 12 plots the thermal contact resistance of Al metallization/emitter Mo and the equivalent surface roughness parameters, σ_{eq} , m_{eq} , and λ_{eq} . It shows a clear relationship between the thermal contact resistance and the surface morphology. In the initial stage, which spans from 0 to 100 k cycles, the σ_{eq} , m_{eq} and λ_{eq} increase by 3.005%, 7.851%, and 4.767%, respectively, indicating a relatively small growth rate. Thus, there is no significant change in the thermal contact resistance of Al metallization/emitter Mo interface. With the increase in the power cycling time from 100 k cycles to 250k cycles, the

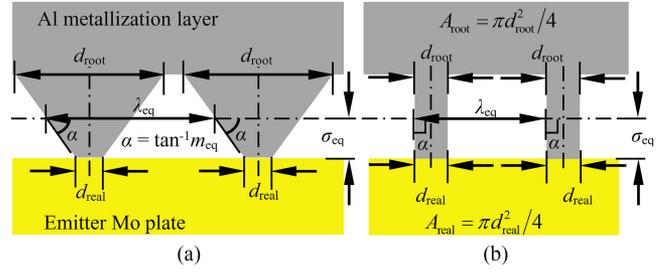


Fig. 13. Definition of the surface morphology parameters of the third-level submodel. (a) $\alpha < 90^\circ$. (b) $\alpha = 90^\circ$.

σ_{eq} , m_{eq} and λ_{eq} increase by 39.297%, 7.184%, and 12.530%, respectively, showing that the σ_{eq} increases rapidly, followed by the λ_{eq} , and the growth rate of m_{eq} almost the same as that before 100 k cycles. As a result, the large σ_{eq} cause a significant increase in the thermal contact resistance, from 0.02339 to 0.02965 K/W, which is a 26.764% increase. For power cycling from 250 k cycles to 400 k cycles, the σ_{eq} , m_{eq} and λ_{eq} increase by 17.053%, 8.937%, and 5.945%, respectively, indicating the changes in σ_{eq} , m_{eq} and λ_{eq} are slower, and thus the thermal contact resistance increases relatively slowly.

During the power cycling, the variations of the σ_{eq} , m_{eq} , and λ_{eq} for the Al metallization/emitter Mo interface occur simultaneously, and thus, the influencing of each parameter is difficult to be examined experimentally. Consequently, to clearly understand the influence of the surface morphology parameters on the thermal contact resistance of the Al metallization/emitter Mo interface, a fractional factorial design analysis based on FE simulations was performed.

As shown in Fig. 13, five factors with two levels examined in this statistical experiment are: A—the relative real contact area (real area A_{real} /apparent area A_{app}); B—the equivalent RMS roughness (σ_{eq}); C—the angle between the asperity and the mean plane ($\alpha = \tan^{-1}m_{eq}$); D—the ratio of the mean spacing between the asperities to the diameter of the root area of the asperities (mean spacing between the asperities λ_{eq} /the diameter of the root area of the asperities d_{root}); and E—the selected location of the third-level submodel, as given in Table VII.

Fully coupled thermal–electrical–structural analysis was performed as introduced in Section III. A total of 16 third-level submodels with different geometric surface topographies were established to investigate the effect of the surface morphology parameters on the thermal contact resistance. The design matrix as well as the FE analysis results are given in Table VII.

Minitab software was used to analyze the results and provided information about the main effects and how these factors interact. Fig. 14 shows the normal probability plot. The points on the line indicate the influence is negligible, while the points away from the line represent a significant effect. Based on this analysis, the main effects of A, C, and D and the BC interactions are the important effects.

The main effects of all factors are plotted in Fig 15(a). The important main effects are A, C, and D, which are the primary

TABLE VII
FACTORIAL DESIGN PLAN AND THE CALCULATED THERMAL CONTACT RESISTANCE

Run	Factor					$R_{th,contact}$ (K/W)
	A	B	C	D	E	
	A_{real}/A_{app} (%)	σ_{eq} (μm)	α (degree)	λ_{eq}/d_{root}	Location of third-level submodel	
1	2	0.5	30	1	corner	0.02359
2	2	0.5	30	4	center	0.01864
3	2	2.5	30	4	corner	0.01687
4	2	2.5	30	1	center	0.01967
5	2	0.5	90	1	center	0.02352
6	2	0.5	90	4	corner	0.01825
7	2	2.5	90	4	center	0.02136
8	2	2.5	90	1	corner	0.02647
9	1	0.5	30	4	corner	0.02254
10	1	0.5	30	1	center	0.02667
11	1	2.5	30	1	corner	0.02607
12	1	2.5	30	4	center	0.02268
13	1	0.5	90	1	corner	0.02979
14	1	0.5	90	4	center	0.02598
15	1	2.5	90	4	corner	0.03125
16	1	2.5	90	1	center	0.03853

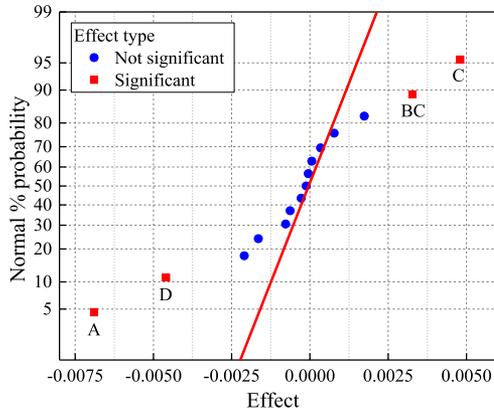


Fig. 14. Normal probability plot of the effects.

factors of interest in this experiment, and the main effects of B and E are not significant. Besides, the main effects of B and C do not represent substantial meaning since they are involved in significant interactions. As expected, factor A has a large negative effect, thereby indicating that a larger A_{real} results in a lower thermal contact resistance. Note that the factor D has a negative main effect; that is, a large λ_{eq} results in low thermal contact resistance. This can be explained by Fig. 16. When the ratio λ_{eq}/d_{root} is equal to 4, the thermal coupling effects between the asperities are negligible because no significant temperature variation can be observed in the region between the asperities. Thus, the values for the heat flux of the asperities are totally independent of each other. As the ratio λ_{eq}/d_{root} is reduced to 1, the thermal coupling effect exists between the asperities, as shown in Fig. 16(b). The heat fluxes cancel each other out in the region between two asperities, and thus, the thermal coupling effect produces a lower heat flux and results in a larger thermal resistance. The factor E has negative

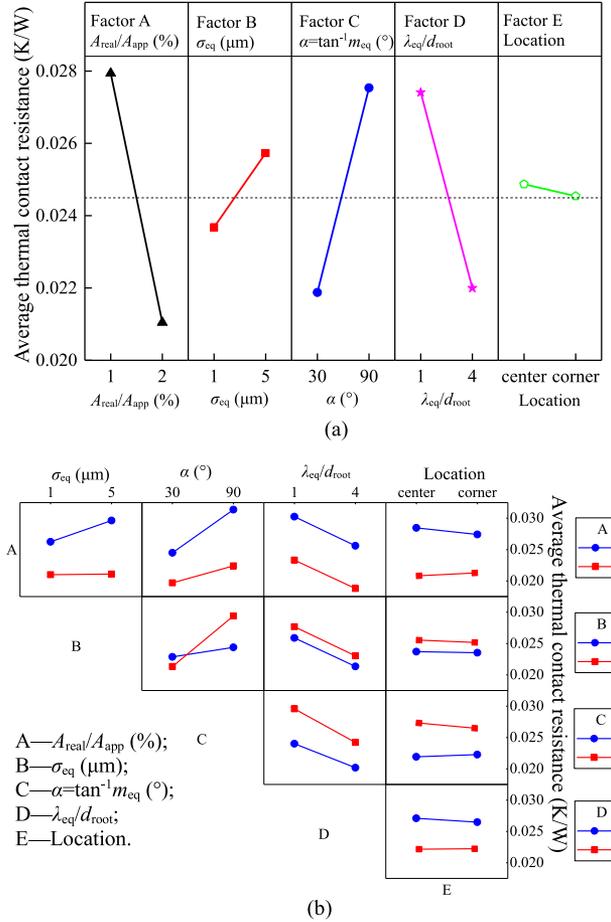


Fig. 15. (a) Main effects and (b) interaction of the surface morphology parameters on the thermal contact resistance.

main effect; that is, the thermal contact resistance is lower in the corner of the PP-IGBT chip than that in the central area. This can be attributed to the nonuniform distribution of the pressure across the PP-IGBT chip. The emitter Mo plate has a smaller area than the PP-IGBT chip, and thus geometric changes cause stress concentration at the edges of the contact surface between PP-IGBT chip and emitter Mo plate. As a result, a lower thermal contact resistance can be achieved in the corner of the PP-IGBT chip where the contact pressure is relatively high.

Fig. 15(b) presents plots of the interactions. Note that all lines except BC are approximately parallel, indicating a lack of interaction between factors. For the response data against factor B for both levels of factor C, the lack of parallelism of the lines suggests an obvious interaction. The BC interaction indicates that if the m_{eq} is high, e.g., the angle between the asperity and the mean plane, α is equal to 90° , an increase in the σ_{eq} , which gives rise to a large separation distance between the contact interfaces of the heat transfer, results in higher values of thermal contact resistance. When the m_{eq} is low, e.g., the angle α is 30° , the root area of the asperities (A_{root} in Fig. 13) will be raised considerably by increasing the σ_{eq} , and thus, heat flow through the asperities increases and the thermal contact

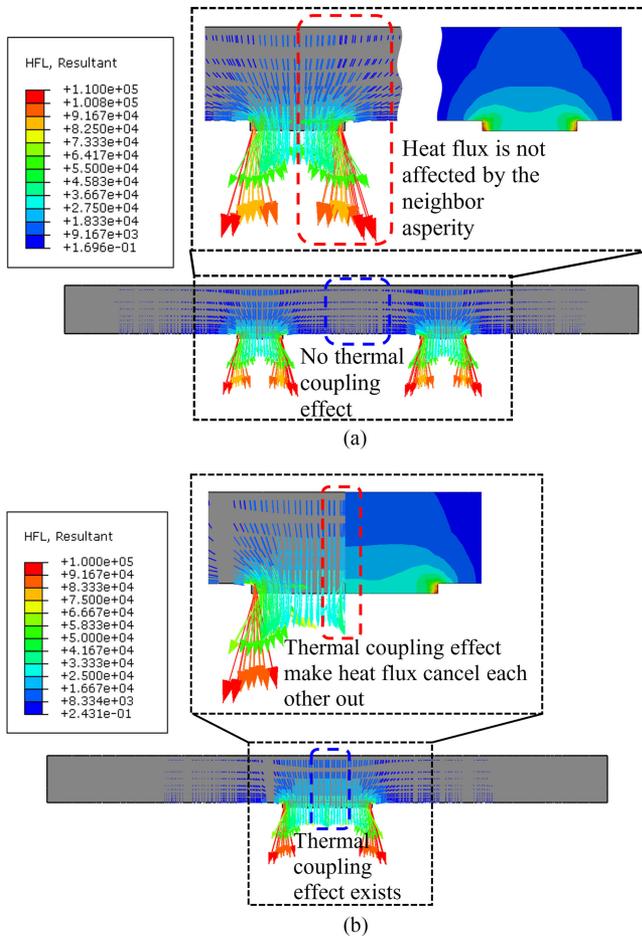


Fig. 16. Heat flux distribution of the Al metallization layer. (a) Run 7, $\lambda_{eq}/d_{root} = 4$. (b) Run 8, $\lambda_{eq}/d_{root} = 1$.

resistance decreases. Additionally, the effect of the m_{eq} is small when the σ_{eq} is at a low level, and the effect of the m_{eq} is large when the σ_{eq} is at a high level. This can be explained by the fact that assuming the real contact area remains unchanged, when the σ_{eq} is large, increasing the m_{eq} means the A_{root} is reduced. Thus, when the heat is transferred from the Al metallization layer into the emitter Mo plate, the dramatic reduction in the area causes heat crowding near the root of the asperities, thereby resulting in that the heat flow experiences a relatively large thermal resistance passing through the asperities. Note from the BC interaction that a low thermal contact resistance would appear to be obtained when the m_{eq} is at a low level and the σ_{eq} is at a high level.

V. CONCLUSION

In this article, the influence of the surface roughness characteristics of the contact interface on the thermal contact resistance of a PP-IGBT module was investigated by experimental observation and FE simulation-based factorial design analysis. The power cycling tests were carried out on PP-IGBT modules. The transient thermal impedance curves of the PP-IGBT modules were measured at different power cycling aging times, and then the thermal contact resistances between

contact interfaces within PP-IGBT modules were estimated with thermal structure functions. The results show that the thermal resistance of the material layer within the PP-IGBT module has little change after power cycling, while the thermal contact resistance, especially the Al metallization/emitter Mo interface, experiences a relatively large increase during power cycling.

The surface morphology changes of the contact interface formed by the Al metallization layer and the emitter Mo plate subjected to power cycling were measured quantitatively and characterized by three parameters: the equivalent RMS roughness σ_{eq} , the equivalent RMS asperity slope m_{eq} , and the equivalent mean spacing between asperities λ_{eq} . The σ_{eq} continually increase during power cycling, and the m_{eq} and the λ_{eq} increase slightly. Additionally, the surface roughening in the corner area is more obvious because the fretting wear at the corner is more serious than that at other locations.

The results of the factorial analysis show that the main effects of the real contact area and the spacing between the asperities, and the interaction of the RMS roughness and the asperity slope have a significant effect on the thermal contact resistance. The main effects indicate that lower thermal contact resistance can be achieved by increasing the real contact area or increasing the spacing between the asperities. The interaction indicates that low thermal contact resistance can be obtained when the asperity slope is small, and the RMS roughness is large.

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and macromechanical behaviors of packaging materials.



and substitution, reliability of semiconductor device and failure mechanism of power semiconductor device.



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