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Comparative Study of the Parameter Acquisition Methods for the Cauer Thermal Network Model of an IGBT Module

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Abstract: Under the operating conditions of high power and high switching frequency, an insulated gate bipolar transistor (IGBT) chip can produce relatively large power loss, causing the junction temperature to rise rapidly; consequently, the reliability of the IGBT module can be seriously affected. Therefore, it is necessary to accurately predict the junction temperature of the IGBT chip. The resistance capacitance (*RC*) thermal network model is a commonly used method for IGBT junction temperature prediction. In this paper, the model parameters are obtained by two methods to establish the Cauer thermal network models of the IGBT module. The first method is to experimentally obtain the transient thermal impedance curve of the IGBT module and the structure function and then extract the individual thermal parameters of the Cauer thermal network model; the second method is to obtain the thermal parameters of the thermal network model directly by using theoretical formulas that consider the influence of the heat spreading angle. The predicted junction temperatures of the Cauer thermal network models established by the two methods are compared with the junction temperatures obtained from infrared (IR) measurements during the power cycling test, the junction temperatures measured by the temperature-sensitive electrical parameter (TSEP) method, and the junction temperatures calculated by finite element (FE) analysis. Additionally, the Cauer thermal network models established by the two methods are compared and verified. The results indicate that the Cauer thermal network model established based on theoretical formulas can accurately predict the maximum junction temperature of the IGBT chip, and the calculated temperature for each layer, from the IGBT chip layer to the ceramic layer, also accords well with the FE results. The Cauer thermal network model established based on the experimental test and the structure function can accurately predict the average junction temperature of the IGBT chip.

Keywords: insulated gate bipolar transistor; junction temperature; Cauer thermal network models

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1. Introduction

Insulated gate bipolar transistors (IGBTs) have become the most important devices in power electronics applications, such as high-power converters, and their reliability directly determines whether the entire system can operate safely and reliably [1,2]. In the service state, the current and voltage of the IGBT module cyclically fluctuate during the turn-on, on-state, and turn-off processes as the working conditions change, causing changes in the power loss of the IGBT chip. The conduction power loss and switching power loss dissipate and generate large amounts of heat, which will increase the junction temperature of the chip. The average junction temperature in the normal service state can reach 60–80 °C, and the junction temperature swing can reach 70–90 °C or even higher [3]. When the IGBT module is operated under working conditions with large junction temperature fluctuations, each material layer can repeatedly undergo thermal expansion and cooling shrinkage. The coefficient of thermal expansion (CTE) of each layer is different [4], and this thermal

mismatch may cause each layer to be repeatedly subjected to thermal stress, causing damage to the material and structure and resulting in degradation in the electrical and heat transfer characteristics of the IGBT module [5], thus eventually leading to bond wire liftoff and solder layer delamination and causing IGBT module failure [6]. Studies have demonstrated that approximately 55% of the failures of electronics are caused by temperature rise [7], and the failure probability of the IGBT module increases sharply with increasing temperature; i.e., for every 10 °C increase in temperature, the failure probability doubles [8]. Because the junction temperature greatly affects the reliability of the IGBT module, accurately predicting the junction temperature of the IGBT module in the service state is of great practical value for ensuring the long-term safe operation of the IGBT module [9].

At present, many advanced methods have been introduced for the junction temperature estimation of the high-power IGBT module. The main experimental methods for obtaining the junction temperature of the IGBT module include optical measurements, physical contact measurements, and temperature-sensitive electrical parameters (TSEPs) [10–13]. Simulation tools have been applied for thermal behavior analysis of the IGBT module, such as the finite element (FE) method [14–16]. FE analyses can obtain the temperature field of the entire IGBT module, but they normally require massive calculations, and it is difficult to be implemented in real mission profiles. FE analyses can obtain the temperature field of the entire IGBT module, but they require a long calculation time. Additionally, resistance capacitance (RC) thermal network models have been widely used for junction temperature calculation of IGBT modules [17]. RC thermal network models are based on thermal–electrical analogy theory; they convert thermal parameters into electrical parameters, integrate the parameters into circuit simulation software, can rapidly calculate IGBT module junction temperatures, and have a wide range of applications [18,19].

The commonly used *RC* thermal network models include the Foster thermal network model and the Cauer thermal network model. The thermal parameters (thermal resistance and thermal capacitance) of the Foster thermal network model are relatively easy to obtain. The commonly used method is to calculate the transient thermal impedance curve of the IGBT module by using FE analysis and to obtain the thermal parameters of the Foster thermal network model by directly fitting the curve [20–22]. In addition, based on the thermal parameters given by the IGBT module supplier, the Foster thermal network model can also be directly established [23]. One shortcoming of the Foster thermal network model is that only the junction temperature and the baseplate temperature can be obtained, whereas the temperature of each material layer within the IGBT module cannot be obtained.

Since the thermal parameters of each layer of the Cauer thermal network model are needed, obtaining the parameters of the Cauer thermal network model is more difficult than obtaining those of the Foster thermal network model. One of the methods currently used is to obtain the thermal resistance and thermal capacitance of each material layer through theoretical calculations based on the geometric dimensions and material parameters of each layer of the IGBT module [24,25]. Some scholars have used this theoretical calculation to obtain parameters to establish a Cauer thermal network model of the press-pack IGBT (PP-IGBT) module and verified the established model by comparing the results with the experimental and FE results [26,27]. In addition, some researchers have obtained the parameters of each layer by analyzing the structure function of the transient thermal impedance curve and established the Cauer thermal network model of the PP-IGBT module [28]. The greatest advantage of the Cauer thermal network model is that the temperature of each material layer of the IGBT module can be obtained.

In this paper, the Cauer thermal network model of the IGBT module is established using two methods: obtaining the model parameters based on the experimentally obtained transient thermal impedance curves and structural functions and obtaining the model parameters based on theoretical calculation. The junction temperatures calculated by the Cauer thermal network models are compared with the junction temperatures obtained from infrared (IR) measurements, the junction temperatures measured by the TSEP method, and the junction temperatures calculated by FE analysis; additionally, the characteristics,

advantages, and disadvantages of the two methods of building the Cauer thermal network model are analyzed.

2. IGBT Module Structure and Heat Transfer Process

2.1. IGBT Module Structure for the Experiment

As shown in Figure 1, a half-bridge IGBT module with a rated voltage of 1200 V and a rated current of 450 A is selected. An IGBT module contains six IGBT chips and six freewheel diode (FWD) chips and has upper and lower bridge arms. Each bridge arm contains three IGBT chips, and one IGBT chip is connected reverse parallel to one FWD chip. All chips are soldered on three direct bonding copper (DBC) ceramic baseplates, an Al metallization layer is sputtered on the surface of the chip, and electrical interconnection to the upper Cu layer of the DBC is achieved via nine Al bond wires. The DBC is connected to the Cu baseplate through a solder layer. In addition, the IGBT module includes protective structures, such as lead-out terminals, silicone gel, and a baseplate.

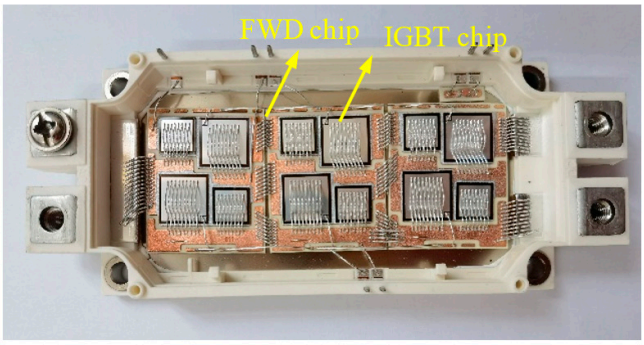


Figure 1. IGBT module to be tested.

2.2. Simplification of the Heat Transfer Process of the IGBT Module

(1) The heat dissipation process considers the heat conduction process only from the chip to the heat sink.

In the service state, the chips in the IGBT module are the main heat source. For the heat generated in the IGBT module, heat conduction is the main heat transfer mechanism, while after reaching the heat sink, the heat diffuses to the external environment in the forms of thermal convection and thermal radiation, as shown in Figure 2. Since the silicone gel on the upper surface of the IGBT module has a good thermal insulation performance, the convective heat transfer on the surface can be ignored. In addition, the junction temperature of the IGBT module generally does not exceed 150 °C, and the thermal radiation can also be ignored. Therefore, the heat dissipation process of the IGBT module considers the heat conduction process only from the IGBT chip to the heat sink, and the heat dissipation on the module's surface and side is ignored [18,22].

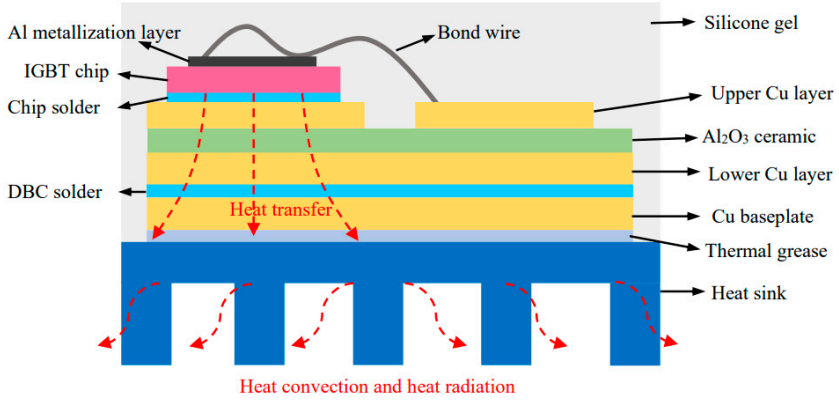


Figure 2. Schematic diagram of the heat transfer process of the IGBT module.

(2) The three-dimensional heat conduction problem of the IGBT module is simplified to a one-dimensional heat conduction problem.

To use the lumped-parameter method to simplify the three-dimensional heat conduction problem of the IGBT module to a one-dimensional heat conduction problem, it is necessary to satisfy certain requirements; i.e., the thermal conductivity of the object is large, the surface area is large, the surface convection heat transfer coefficient is very small, the thickness is very low, and the thermal resistance inside the object is negligible compared to the convective heat transfer resistance of the surface. Then, the Biot number, Bi, is introduced:

$$Bi = \frac{hl}{\lambda} < 0.1M \tag{1}$$

where h is the convective heat transfer coefficient on the surface of the object, l is the thickness of the object, λ is the thermal conductivity of the object, and M is a constant related to the geometric shape of the object. For infinite flat plates, $M = 1$; for infinitely long cylinders and square columns, $M = 1/2$; and for spheres and cubes, $M = 1/3$. In general, because each layer in the IGBT module is very thin (that is, l is very small), each layer can be regarded as an infinite plate, and $M = 1$. The convective heat transfer on the surface of the IGBT module can be ignored; consequently, h is small. Therefore, for each layer of the IGBT module, $Bi < 0.1$, which satisfies the applicable condition of the lumped-parameter method [29], and the one-dimensional heat conduction equation can be used to describe the heat conduction process inside the IGBT module.

(3) The thermal coupling effect between IGBT chips is ignored.

In the direct current (DC) power cycling test, only the upper half of the IGBT module is connected to the circuit, and the FWD chips do not work; that is, only three IGBT chips work at the same time. The upper copper layer of the IGBT module is three separate pieces of copper instead of one piece of copper. Such structure features will reduce the coupling effect between IGBT chips. Additionally, studies have demonstrated that when the distance between two chips is greater than 10 mm, the thermal coupling effect between them can be ignored [30]. The distance between the IGBT module chips used in this paper is 19 mm; therefore, under the DC power cycling test, the thermal coupling effect between chips can be ignored.

In summary, to calculate the junction temperature of an IGBT chip, only the vertical thermal path must be considered.

3. Modeling Process of the *RC* Thermal Network Model of the IGBT Module

3.1. Cauer Thermal Network Model Structure

A one-dimensional Cauer thermal network model for the IGBT module is established, as shown in Figure 3. The established *RC* thermal network model has a heat flow path, which contains seven *RC* units, corresponding to the IGBT module's seven-layer structure, consisting of the IGBT chip, the chip solder layer, the upper Cu layer of the DBC, the ceramic layer of the DBC, the lower Cu layer of the DBC, the DBC solder layer, and the Cu baseplate layer. The Cauer thermal network model contains RC units, which are corresponding to the IGBT module's material layers, and thus, the temperature of all the material layers within the IGBT module can be obtained. Here, to obtain the temperature results of some material layers that cannot be obtained, the order reduction techniques were not applied [31]. In the thermal–electrical analogy method, the heat transfer process in the IGBT module is analogous to the electrical conduction process by treating temperature T, heat flow P, thermal resistance R_{th}, and thermal capacitance C_{th} as voltage U, current I, resistance R_{el}, and capacitance C_{el}, respectively. An equivalent circuit model is established in the circuit simulation software to analyze the thermal conduction characteristics of the IGBT module, and the obtained node voltage between each *RC* unit is the temperature of each layer.

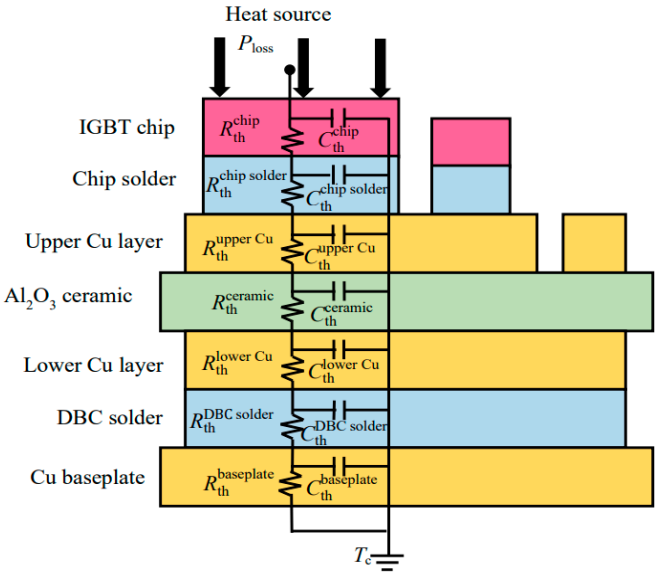


Figure 3. Cauer thermal network model of the IGBT module.

3.2. Determining the Parameters of the RC Thermal Network Model by Using the Transient Thermal Impedance Curve Test and Structure Function

First, the *K* curve is obtained through experiments. Before the experiment, a calibration test is performed to obtain the relationship between the on-state collector–emitter voltage drop ($V_{ce\text{-}on}$) and the junction temperature (T_j), i.e., the *K* curve. A thermostat experimental device is used to obtain the $V_{ce\text{-}on}$ of the device under test (DUT) under different T_{js}, the curve of T_j and $V_{ce\text{-}on}$ is plotted, and the *K* curve is obtained by fitting the data. The results are shown in Figure 4, and the *K* factor of the IGBT module is −2.35 mV/°C.

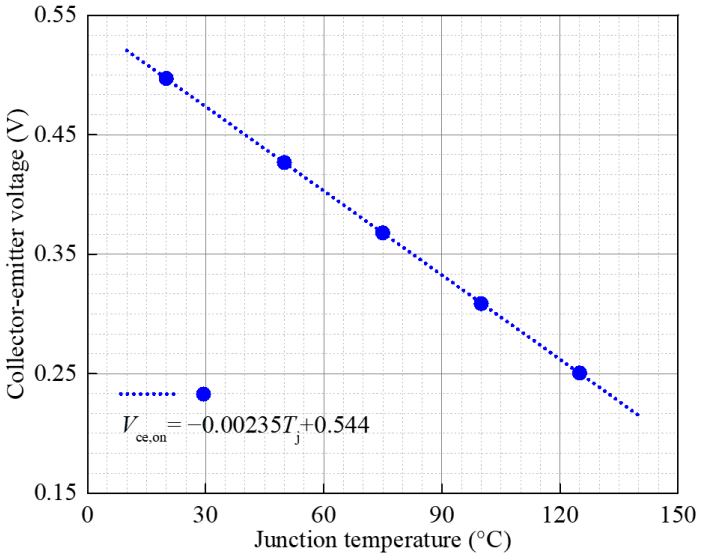


Figure 4. The calibration curve of the $V_{ce\text{-}on}$ and T_j of the IGBT module.

Then, the T3Ster thermal resistance tester is used to measure the transient thermal impedance curve of the IGBT module. The configuration of the transient thermal impedance curve measurement is shown in Figure 5. When the transient thermal impedance curve test starts, a heating current of 100 A flows through the DUT for a heating time of 200 s. The IGBT module is heated to thermal equilibrium, the heating current is turned off, and water cooling is started. At this time, the test current is applied to the circuit to measure the $V_{ce\text{-}on}$ of the DUT in the cooling stage, and the sampling interval is 1 µs. The $T_j(t)$ during

the cooling process is calculated using the K curve. Then, from the $T_j(t)$ and the heating power P, the transient thermal impedance curve $Z_{th,\,cooling}(t)$ during the cooling process can be obtained, as shown in Figure 6.

$$Z_{th,cooling}(t) = \frac{T_j(t) - T_j(t=0)}{P} \tag{2}$$

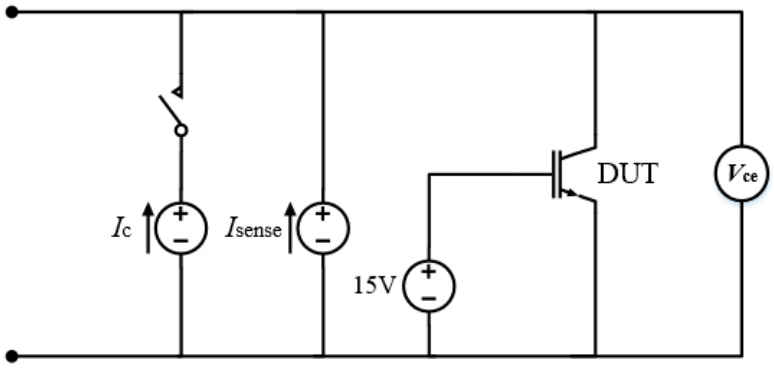


Figure 5. Configuration of the transient thermal impedance curve test.

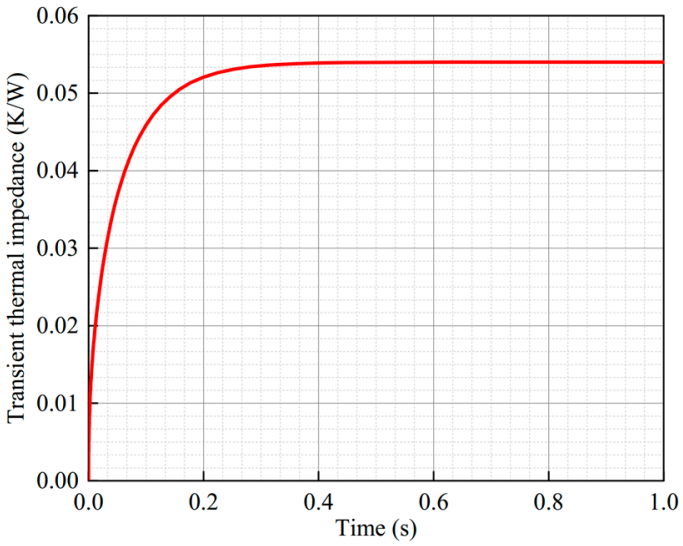


Figure 6. Transient thermal impedance curve.

The cumulative structure function $C(R_{th})$ and differential structure function $\rho(R_{th})$ are obtained by mathematical transformations of the transient thermal impedance curve, such as numerical derivation and deconvolution.

$$C(R_{th}) = c \cdot \rho \cdot \lambda \cdot A^2 \cdot R_{th} \tag{3}$$

$$\rho(R_{th}) = \frac{dC(R_{th})}{R_{th}} = c \cdot \rho \cdot \lambda \cdot A^2 \tag{4}$$

where R_{th} is the thermal resistance, c is the specific heat capacity of the material, ρ is the material density, λ is the thermal conductivity of the material, and A is the effective heat transfer area.

The cumulative structure function and the differential structure function can provide the thermal resistances and thermal capacitances of the material layers within the IGBT module. According to the cumulative structure function (Equation (3)), when the heat

transfer area of a certain material layer changes or the heat enters one material layer from another material layer, the slope of the cumulative structure function curve may change. As shown in Equation (4), the differential structure function is the derivative of the cumulative structure function on the thermal resistance; that is, at the same position, the change in the slope of the cumulative structure function curve could lead to the extreme value of the differential structure function curve. According to this feature, the thermal resistance and thermal capacitance of each material layer can be determined by dividing the cumulative and differential structure function curves. Figure 7 shows the cumulative structure function and differential structure function curves of the IGBT module. Based on the structure function, the thermal resistance R_{th} and the thermal capacitance C_{th} of each material layer of the tested IGBT module are obtained, as shown in Table 1.

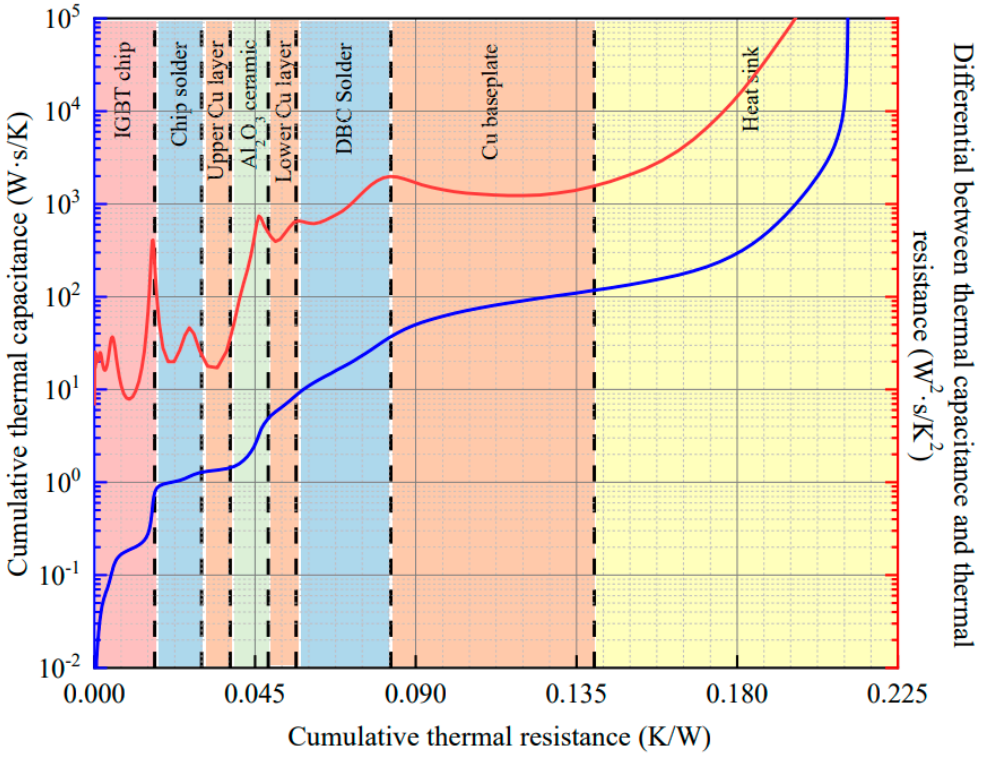


Figure 7. Cumulative and differential structure functions of the IGBT module.

Table 1. The thermal resistance and thermal capacitance of each layer of the IGBT module obtained based on the experimental test and the structure function.

Each Layer	R_{th}/(°C/W)	C_{th}/(J/°C)
IGBT chip	0.0169	0.8542
Chip solder	0.0131	0.4032
Upper Cu layer on the DBC	0.008	0.1377
DBC ceramic layer	0.0107	3.3457
Lower Cu layer on the DBC	0.0078	3.5861
DBC solder	0.0265	28.199
Cu baseplate	0.057	79.772

3.3. Determining the Parameters of the RC Thermal Network Model by Using Theoretical Formulas

The thermal resistance R_{th} and the thermal capacitance C_{th} of each layer can be calculated according to the following equation:

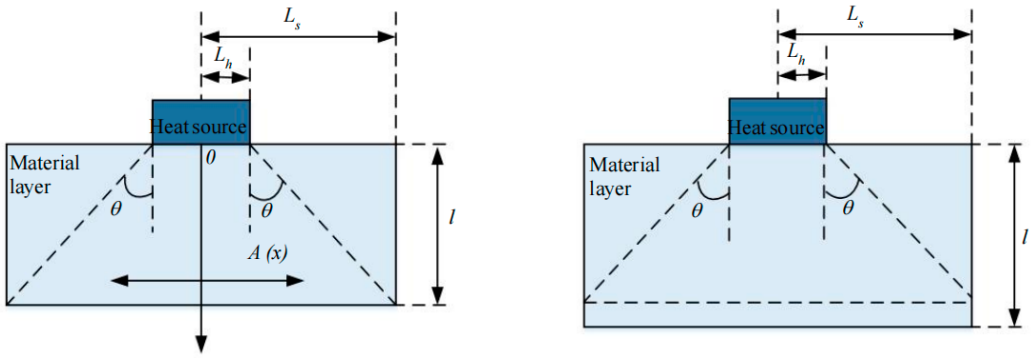
$$R_{th} = \frac{l}{\lambda A} \tag{5}$$

$$C_{\mathrm{th}} = c\rho Al \tag{6}$$

where λ is the thermal conductivity of each material layer, A is the effective heat transfer area of each layer, c is the specific heat capacity of each layer, ρ is the density of each layer, and l is the thickness of each layer. The effective heat conduction area A is one of the key factors affecting the thermal resistance and thermal capacitance of each layer.

In the IGBT module, the heat generated by the IGBT chip not only diffuses in the vertical direction but also laterally diffuses when the area of the heat source is small; that is, the effective heat conduction area can gradually expand [32,33], as shown in Figure 8. Here, it is assumed that the heat source is a square, where L_{h} is the 1/2 side length of the heat source, L_{s} is the 1/2 side length of the layer for determining the thermal capacitance and thermal resistance, l is the thickness of the layer, and θ is the heat spreading angle ($0 < \theta < 90°$). When calculating the effective heat transfer area, the two cases of $l \le (L_{\mathrm{s}} - L_{\mathrm{h}})/\tan\theta$ and $l > (L_{\mathrm{s}} - L_{\mathrm{h}})/\tan\theta$ must be considered. As shown in Figure 8a,b, the effective heat conduction area at any point x in the coordinate system is

$$\begin{cases} A(x) = 4(L_{\mathrm{h}} + x\tan\theta)^2 & x \le l \le \frac{L_{\mathrm{s}}-L_{\mathrm{h}}}{\tan\theta} \\ A(x) = 4{L_{\mathrm{s}}}^2 & \frac{L_{\mathrm{s}}-L_{\mathrm{h}}}{\tan\theta} < x \le l \end{cases} \tag{7}$$



(a) $l \le (L_s\text{-}L_h)/\tan\theta$ **(b)** $l > (Ls\text{-}L_h)/\tan\theta$

Figure 8. Lateral diffusion of heat from the heat source.

Substituting Equation (7) into Equations (5) and (6) and integrating along the thickness of the layer, we have

$$\begin{cases} R_{\mathrm{th}} = \int_0^{\frac{L_{\mathrm{s}}-L_{\mathrm{h}}}{\tan\theta}} \frac{\mathrm{d}x}{4\lambda(L_{\mathrm{h}}+x\tan\theta)^2} + \int_{\frac{L_{\mathrm{s}}-L_{\mathrm{h}}}{\tan\theta}}^{l} \frac{\mathrm{d}x}{4\lambda{L_{\mathrm{s}}}^2} \\ \quad = \frac{1}{4\lambda L_{\mathrm{h}}}\left(\frac{l^*}{L_{\mathrm{h}}+l^*\tan\theta} + \frac{L_{\mathrm{h}}(l-l^*)}{{L_{\mathrm{s}}}^2}\right) \\ C_{\mathrm{th}} = \int_0^{\frac{L_{\mathrm{s}}-L_{\mathrm{h}}}{\tan\theta}} 4c\rho(L_{\mathrm{h}}+x\tan\theta)^2\mathrm{d}x + \int_{\frac{L_{\mathrm{s}}-L_{\mathrm{h}}}{\tan\theta}}^{l} 4c\rho{L_{\mathrm{s}}}^2\mathrm{d}x \\ \quad = \frac{4c\rho}{3\tan\theta}\left[(L_{\mathrm{h}}+l^*\tan\theta)^3 - {L_{\mathrm{h}}}^3\right] + 4c\rho{L_{\mathrm{s}}}^2(l-l^*) \end{cases} \tag{8}$$

where the equivalent thickness l^* is [34]

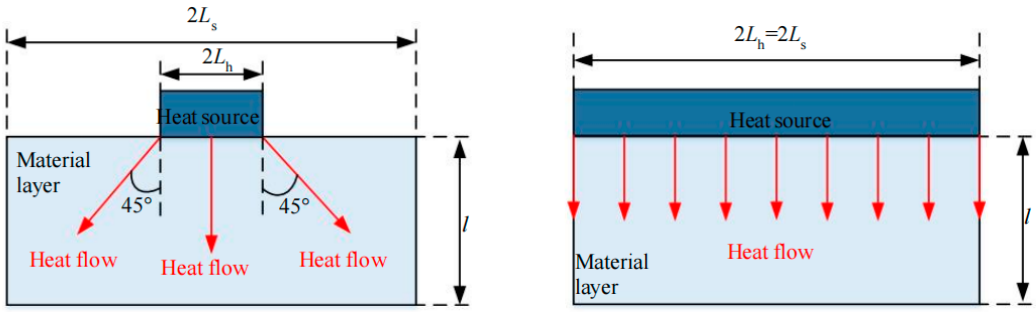
$$l^* = \min\left(\frac{L_{\mathrm{s}} - L_{\mathrm{h}}}{\tan\theta},\ l\right) \tag{9}$$

Equation (8) indicates that the key to calculating the thermal resistance and thermal capacitance is the heat spreading angle. Existing studies take the heat spreading angle as a certain value, such as 45° [35], 32.5° [36], and 26.6° [37], which can meet the requirement when the computational accuracy is low. However, to obtain a more accurate thermal

resistance and thermal capacitance, it is necessary to further consider the influence of the lateral boundary effect and the vertical boundary effect on the heat spreading angle.

First, the influence of the lateral boundary effect on the heat spreading angle is analyzed; this influence refers mainly to the influence of the lateral dimension of the layer. In Figure 9a, when $L_h/L_s << 1$, the area of the heat source is much smaller than the area of the layer, and the heat spreading angle in the layer is 45°; i.e., $\tan\theta = 1$. In Figure 9b, when $L_h/L_s = 1$, the area of the layer is equal to the area of the heat source, and the heat spreading angle in the baseplate is 0°; that is, $\tan\theta = 0$. Therefore, the influence of the lateral boundary effect on the heat spreading angle can be linearly expressed as follows [34,38]:

$$\tan\theta = 1 - \frac{L_h}{L_s} \qquad 0 < \frac{L_h}{L_s} \le 1 \tag{10}$$



(**a**) $L_h/L_s << 1$ (**b**) $L_h/L_s = 1$

Figure 9. Effect of the lateral boundary effect on the heat spreading angle.

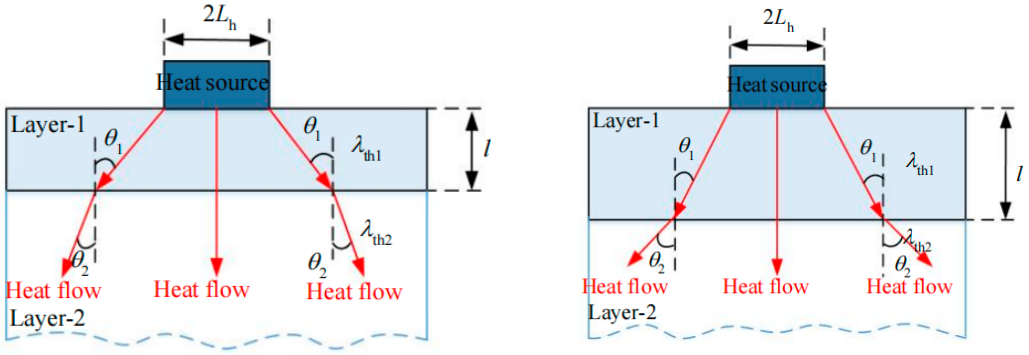
Next, the influence of the vertical boundary effect on the heat spreading angle is analyzed; this influence includes mainly the influence of the layer thickness and the change in the thermal conductivity at the interface of the two layers. In Figure 10a, when $l/L_h << 1$, layer-1 is very thin. If $\lambda_{th1}/\lambda_{th2} \to 0$, i.e., the thermal conductivity of layer-2 greatly exceeds that of layer-1, then layer-2 can be regarded as an isothermal boundary, and thus, the heat spreading angle in layer-1 is 0°; i.e., $\tan\theta_1 = 0$. If $\lambda_{th1}/\lambda_{th2} \to \infty$, the thermal conductivity of layer-2 is much smaller than that of layer-1, and layer-2 can be regarded as an adiabatic boundary, and thus, the heat spreading angle in layer-1 is 90°; i.e., $\tan\theta_1 \to \infty$. If $\lambda_{th1}/\lambda_{th2} = 1$, i.e., the thermal conductivity of layer-2 is equal to that of layer-1, the heat spreading angle in layer-1 is 45°; i.e., $\tan\theta_1 = 1$. In Figure 10b, when $l/L_h >> 1$, the thermal conductivity of layer-2 has no effect on the heat spreading angle in layer-1, and the heat spreading angle in layer-1 is 45°; i.e., $\tan\theta_1 = 1$. Therefore, the influence of the vertical boundary effect on the heat spreading angle can be expressed as [34]

$$\tan\theta = \frac{l + L_h\lambda_{th}'/(1+\lambda_{th}')}{l + L_h/(1+\lambda_{th}')} \tag{11}$$

where $\lambda_{th}' = \lambda_{th1}/\lambda_{th2}$ is the thermal conductivity ratio.

Finally, by combining Equations (10) and (11), the heat spreading angle equation that comprehensively considers the effects of the structural size and thermal conductivity of the IGBT module is obtained:

$$\tan\theta = \frac{l + L_h\lambda_{th}'/(1+\lambda_{th}')}{l + L_h/(1+\lambda_{th}')}\left(1 - \frac{L_h}{L_s}\right) \tag{12}$$



(**a**) $l/L_h << 1$ (**b**) $l/L_h >> 1$

Figure 10. Effects of the vertical boundary on the thermal spreading angle.

According to the structural dimensions and material parameters of the IGBT module, the thermal resistance R_{th} and the thermal capacitance C_{th} of each layer are obtained from Equations (8) and (12), as shown in Table 2.

Table 2. Theoretically calculated thermal resistance and thermal capacitance of each layer in the IGBT module.

Material Layer	Length (mm)	Width (mm)	Thickness (μm)	R_{th} (°C/W)	C_{th} (J/°C)
IGBT chip	13.5	13.5	140	7.41×10^{-3}	5.94×10^{-2}
Chip solder	13.5	13.5	150	1.44×10^{-2}	4.59×10^{-2}
Upper Cu layer on the DBC	30.0	14.5	300	3.94×10^{-3}	0.19
DBC ceramic layer	40.0	32.0	380	9.07×10^{-2}	0.24
Lower Cu layer on the DBC	38.0	30.0	380	4.09×10^{-3}	0.30
DBC solder	38.0	30.0	300	2.08×10^{-2}	0.13
Cu baseplate	122.0	62.0	3000	2.08×10^{-2}	3.79

Based on the established Cauer thermal network model and the calculated power losses under DC conditions, the *RC* thermal network model is established in MATLAB/Simulink, and the junction temperature of the IGBT chip and the temperature of each layer are calculated.

4. Experimental Measurement of the IGBT Chip Junction Temperature

To verify and compare the accuracy of the junction temperature calculated by the Cauer thermal network model established by the two methods, the TSEPs and the IR measurement methods are used to measure the junction temperature during the power cycling test, and the calculated junction temperature is compared with that obtained from the experiments.

4.1. Power Cycling Test Process

The power cycling test platform is built and includes a main power source, a test power source, a signal generator, a drive and protection circuit, a data acquisition system, an IR camera, and a water-cooling system, as shown in Figure 11. The DC power cycling test is performed. The DUT is installed on a water-cooled heat sink. The drive circuit applies a 15 V drive signal to the gate of the IGBT module to maintain the on-state. When the main circuit is turned on, a constant load current I_c is applied to the IGBT module, and the water-cooling box does not provide cooling water to the heat sink, causing the IGBT module to rapidly heat up. When the main circuit is turned off, the control valve is opened to introduce cooling water to the heat sink to rapidly cool the temperature.

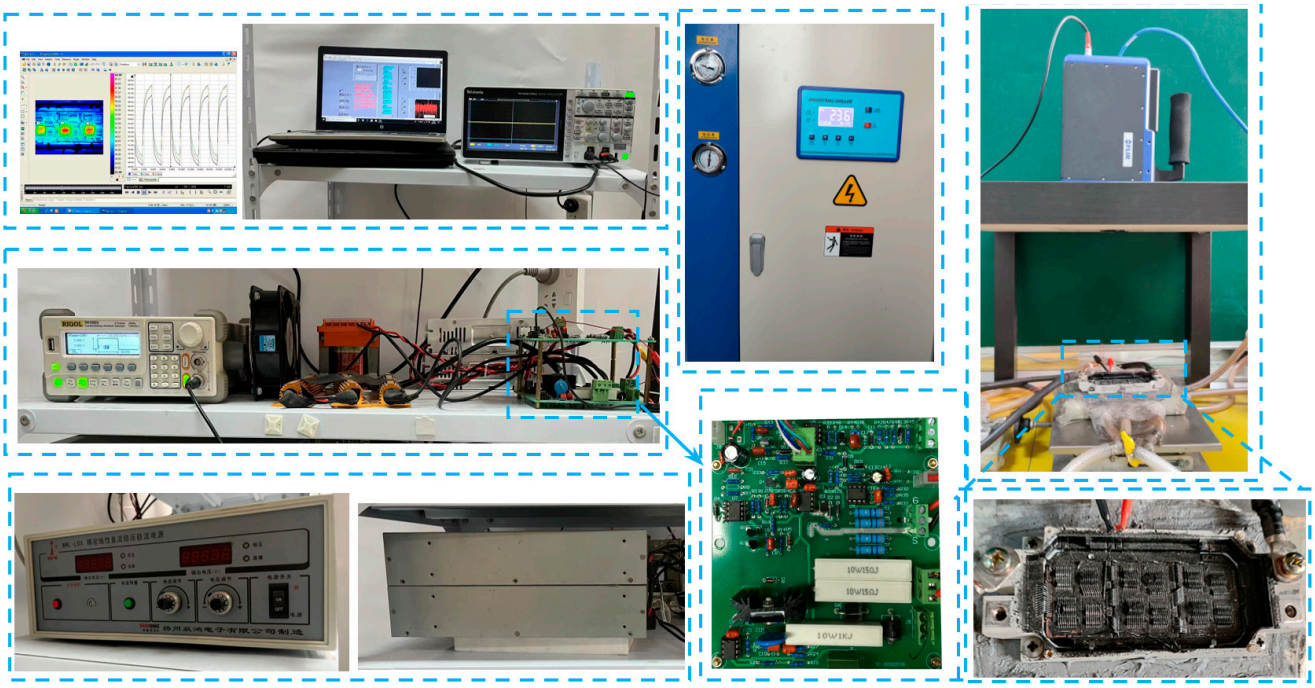
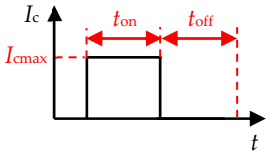


Figure 11. Power cycling test platform.

The conditions of the DC power cycling test are shown in Table 3. The control strategy of fixed turn-on and turn-off time is adopted, and two sets of experiments are conducted. In the first set of experiments, the load current is 140 A, the turn-on and turn-off times are t_{on} = 4 s and t_{off} = 4 s, respectively, and the period is 8 s; in the second set of experiments, the load current is 400 A, the turn-on and turn-off times are t_{on} = 2 s and t_{off} = 2 s, respectively, and the period is 4 s. For the water-cooled heat sink, the constant water temperature is set to 45 °C.

Table 3. Experimental conditions for IR temperature measurement.

Experimental Conditions	Load Current Waveform	I_{cmax} (A)	t_{on}/t_{off} (s)	T_w (°C)
DC-1		140	4/4	45
DC-2		400	2/2	45

I_{cmax} is the peak load current, t_{on}/t_{off} is the turn-on/off time of the main circuit, and T_w is the cooling water temperature.

4.2. Measuring the Junction Temperature by Using the IR Thermal Imaging Method

The FLIR SC7300 M IR camera (Teledyne FLIR, the United States) is used; the resolution of all IR images is 320 × 240, and the sampling frequency is 200 Hz. To facilitate the temperature measurement by the IR camera, a customized IGBT module without silicone gel is used, and a layer of insulating black paint with an emissivity of 0.97 is evenly sprayed on the internal surface of the module to reduce the error of IR temperature measurement.

To capture the minimum and maximum junction temperatures of the IGBT chips at the turn-on and turn-off moments, it is necessary to correspond the time in the power cycling test to the temperature distribution image captured by the IR camera. In this experiment, an external signal is used to control the IR camera, and the synchronization of the trigger signal with the switch signal is also archived; i.e., the signal generator outputs two signals, one of which provides the driving voltage for the main circuit switch to control the on/off of the main circuit, while the other is used to trigger the IR camera to measure the temperature

field. Synchronizing the switching signal and the trigger signal allows the temperature field image taken by the IR camera to correspond to the time in the power cycling test.

4.3. Measuring the Junction Temperature by Using the TSEPs

The TSEP method measures electrical parameters that have a certain correlation with the junction temperature of the IGBT module, uses the relationship curve between these electrical parameters and the junction temperature, and finally indirectly obtains the junction temperature through conversion [39]. The functional relationship between the $V_{\text{ce-on}}$ of the IGBT module and T_{j} is given in Section 3.2. During the experiment, to measure the maximum junction temperature, when the circuit is turned off, the $V_{\text{ce-on}}$ of the IGBT module at a current of 100 mA is measured, and the junction temperature of the IGBT module is calculated from the $V_{\text{ce-on}} - T_{\text{j}}$ relationship curve at 100 mA.

5. Obtaining the Junction Temperature of the IGBT Module by Using FE Analysis

Because the experimental test can obtain the junction temperature of only the IGBT chip, it is impossible to verify the accuracy of the temperature of other material layers calculated by the Cauer thermal network model. Therefore, an FE model of the IGBT module is developed, electrical–thermal FE analysis is carried out to calculate the layer temperature under the two DC working conditions, and the calculated layer temperature is compared with that obtained by the Cauer thermal network model.

As shown in Figure 12, the three-dimensional FE model of the IGBT module is established. The model includes Al bond wires, an Al metallization layer, an IGBT chip, a diode chip, a chip solder layer, an upper Cu layer, a ceramic layer, a lower Cu layer, a DBC solder layer, and a Cu baseplate. The geometric dimensions of the FE model were the same as that of the test sample.

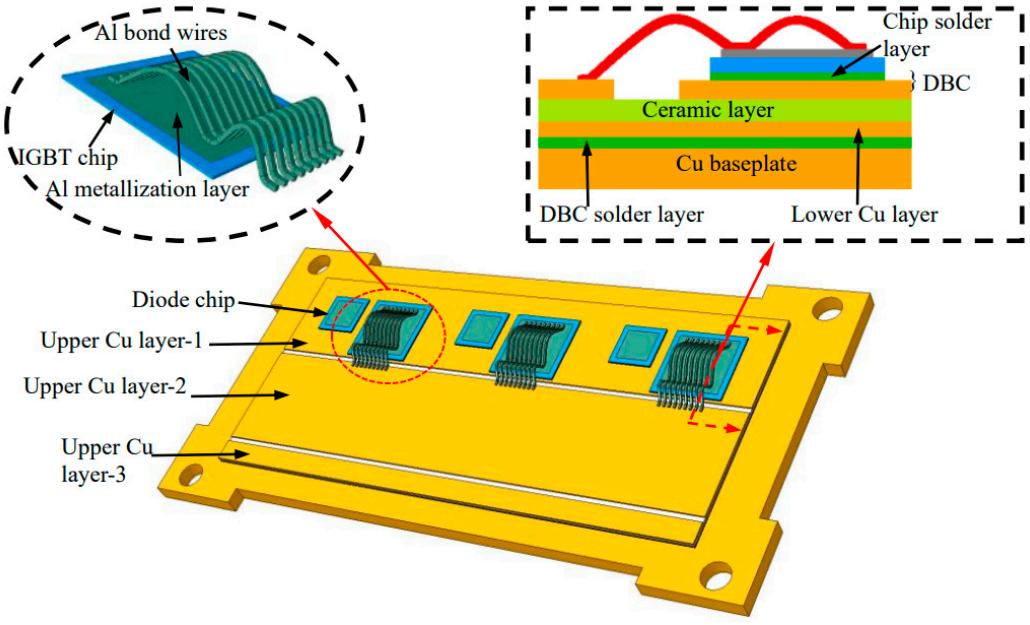


Figure 12. Three-dimensional FE model of the IGBT module.

To obtain the layer temperature of the IGBT module under the DC power cycling test, electrical–thermal analysis is performed. The material parameters used are shown in Table 4. In the electrical–thermal analysis, the eight-node linear brick coupled thermal–electrical element (DC3D8E) is used, and the entire model has 154,146 elements.

Table 4. Material parameters used in electrical–thermal FE analysis.

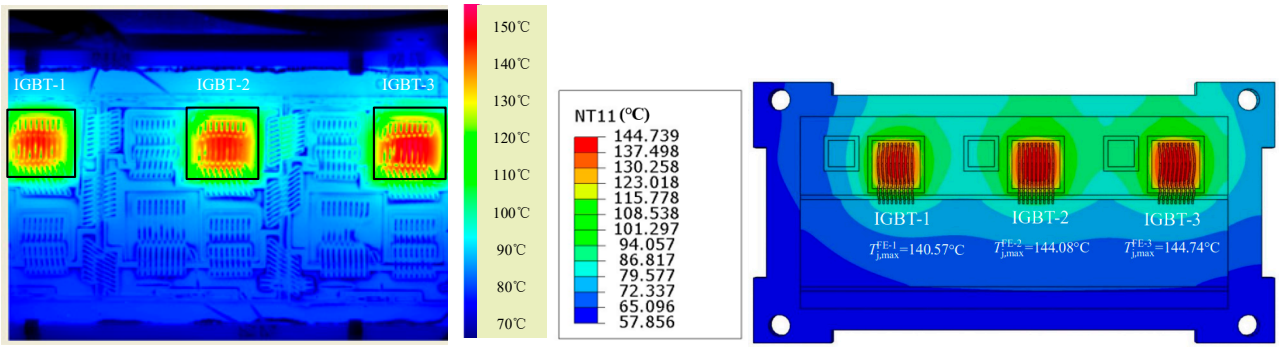
Material	Thermal Conductivity (W/m·K)	Resistivity (mΩ·mm)	Density (kg/m^3)	Specific Heat (J/kg·K)
Al [40]	237	2.65×10^{-2}	2.70×10^3	900
Si [40]	148	7.7×10^3	2.33×10^3	700
SnAgCu305 solder [21]	57	1.04×10^{-1}	7.30×10^3	230
Al_2O_3 [41]	20	1×10^{18}	3.96×10^3	753
Cu [40]	400	1.68×10^{-2}	8.92×10^3	380

In the electrical–thermal FE analysis, the current flows in from the right end of upper Cu layer-1, passes through the IGBT chip and the Al bond wires, and finally flows out from the left end of upper Cu layer-2. The current and initial temperatures are set according to the actual DC power cycling test conditions. At the bottom surface, the convective heat transfer coefficients corresponding to the two power cycling test conditions are set to 650 W/(m^2·K) and 2000 W/(m^2·K).

6. Results and Discussion

6.1. Comparison of Junction Temperatures by Using TSEP, IR Measurement, and FE Analysis

Figure 13a shows the experimental result of the DC-2 test condition. After the IGBT module has reached a stable operating condition, i.e., the heat generation and heat dissipation have reached equilibrium, the temperature field of the IGBT module at the moment when the main circuit is turned off is captured by the IR camera. Similarly, under DC-2 test conditions, the temperature field when the IGBT module reaches the maximum temperature is obtained from the electrical–thermal FE analysis, as shown in Figure 13b. The temperature distribution obtained by FE modeling is consistent with the temperature distribution obtained by IR measurement. The IGBT chip is the main heat source area. The junction temperatures of the three IGBT chips are much higher than the temperatures of the other material layers, and the temperature distribution of the entire IGBT module decreases gradually from the IGBT chip to the edge. On the IGBT chip, a significant temperature gradient can also be observed, with the highest temperature at the center of the chip and the lowest temperature at the edge of the chip.



(**a**) (**b**)

Figure 13. Comparison of the temperature fields of the IGBT module under the DC-2 experimental conditions: (**a**) Infrared image taken by the IR camera of the IGBT module at the moment of power-off; (**b**) The temperature field when the IGBT module reaches the maximum temperature obtained from the electrical–thermal FE analysis.

In addition to the temperature distribution, the maximum junction temperatures obtained by the experiment and the FE analysis are also very close. The highest junction temperatures of the surfaces of the three chips obtained by IR thermal imaging are obtained. Among these temperatures, the junction temperature of IGBT-3, at approximately 147.12 °C,

is the highest; the junction temperature of IGBT-2, at approximately 142.24 °C, is the second highest; and the junction temperature of IGBT-1, at approximately 136.54 °C, is the lowest. According to the FE simulation, the maximum surface temperatures of IGBT-3, IGBT-2, and IGBT-1 are 144.74 °C, 144.08 °C, and 140.57 °C, respectively, which differ from the IR imaging results by −1.62%, 1.29%, and 2.95% (all < 3%), respectively. Therefore, the established FE model can accurately obtain the junction temperature of the IGBT module.

Table 5 gives the junction temperature results estimated by the TSEP measurement, IR camera measurement, and FE analysis. The junction temperature value given by the TSEP measurement is in good agreement with the mean junction temperature obtained with the IR camera measurement. The differences between the junction temperature obtained by the TSEP measurement and the mean junction temperature obtained with the IR camera measurement values of each IGBT chip are less than 2 °C, and the junction temperature obtained by the TSEP measurement value is very representative of the mean junction temperature of the three IGBT chips, with errors lower than 1 °C. The results are in accordance with previous studies, which suggests that the TSEP method can provide an adequate assessment of the mean junction temperature of IGBT chips in a parallel condition. However, a comparison of junction temperature obtained by the TSEP measurement in relation to the peak value obtained by the IR camera measurement for each IGBT chip shows that the junction temperature obtained by the TSEP measurement clearly underestimates the maximum junction temperature of the IGBT chips and gives the results with the largest errors, i.e., more than 5 °C. The error percentage for the maximum junction temperature obtained from the FE analysis relative to that from the IR camera measurement is less than 1%, and such small differences between the results confirm that the convection coefficients and external temperatures are well defined in the FE analysis.

These results suggest that TSEP measurements based on $V_{\text{ce-on}}$ can only provide a mean junction temperature for the IGBT chips and cannot provide the peak junction temperature. The maximum junction temperature can be obtained by an IR camera or FE analysis.

Table 5. Junction temperature measurement results.

	T_j-TSEP (°C)	$T_{j,mean}$-IR Camera (°C)	Error (T_j-TSEP − $T_{j,mean}$-IR Camera) (°C)	$T_{j,max}$-IR Camera (°C)	Error(T_j-TSEP − $T_{j,max}$-IR Camera) (°C)	$T_{j,max}$-FE (°C)	Error($T_{j,max}$-IR Camera − $T_{j,max}$-FE) (°C)
IGBT 1	59.58	59.09	−0.49	64.82	5.24	64.37	0.45
IGBT 2		60.26	0.68	65.11	5.53	65.36	−0.25
IGBT 3		61.09	1.51	66.06	6.48	65.41	0.65
Average		60.15	0.57	-	-	-	-

The IR camera measures the energy of infrared radiation emitted by the object and obtains the surface temperature of the object through calculation and processing, and thus, the IR camera can directly capture the temperature distribution of the IGBT chip surface, and the highest temperature can also be obtained. According to the test principle of the TSEP method, the TSEP method measures the electrical parameter, $V_{\text{ce-on}}$, which has a certain correlation with the junction temperature of the IGBT module, uses the relationship curve between the $V_{\text{ce-on}}$ and the junction temperature, and finally indirectly obtains the junction temperature through conversion. Because the value of $V_{\text{ce-on}}$ is affected by the junction temperature of all chips within the IGBT module, the TSEP method can only obtain the average temperature of the IGBT chip and cannot obtain the maximum temperature. Therefore, the temperature result obtained from the IR measurement is higher than that obtained from the TSEP method.

6.2. Comparison of the Experimental Junction Temperatures and Those Calculated by the RC Thermal Network Models Obtained by the Two Methods

Under the two experimental conditions of DC-1 and DC-2, the predicted junction temperatures of the Cauer thermal network models established by the two modeling methods, i.e., structural function and theoretical calculation, are compared with the junction temperatures measured by the TSEPs and obtained from IR measurement, as shown in Figure 14.

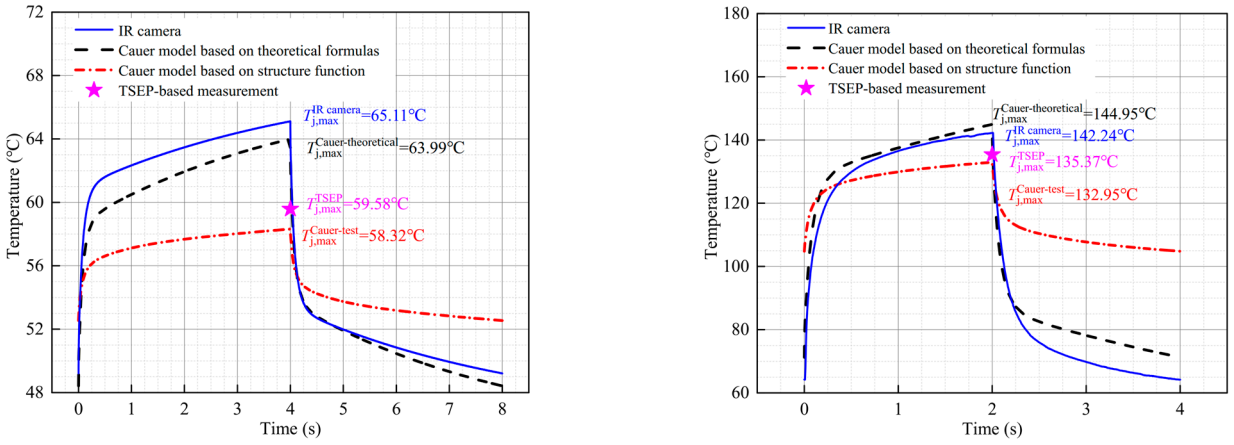


Figure 14. Comparison of the temperatures from the IR camera measurement and the Cauer model analysis for the central region of the IGBT chip: (**a**) Under DC-1 test conditions; (**b**) Under DC-2 test conditions.

Under the DC-1 test condition, the IGBT module's junction temperature measured at the power-off moment by the TSEPs method is 59.58 °C, which is lower than the maximum junction temperature obtained from IR measurement but is very close to the IGBT chip's average junction temperature (60.15 °C) obtained by IR measurement; this temperature represents a difference of only 0.57 °C. Similarly, under the DC-2 experimental conditions, the IGBT module's junction temperature measured at the power-off moment by the TSEP method is 135.37 °C, which is also lower than the IGBT chip's maximum junction temperature obtained by the IR measurement. According to the test principle of the TSEP method, the TSEP method can obtain the average temperature of the IGBT chip only at a certain time and cannot obtain the maximum temperature.

The IR measurement result under the DC-1 test condition is compared with the calculated results of the Cauer thermal network model established by the two methods, as shown in Figure 14a. The maximum junction temperature of the Cauer thermal network model established based on the theoretical calculation is 63.99 °C, which is very close to the maximum junction temperature of 65.11 °C obtained by IR measurement; this temperature represents a difference of approximately 1.12 °C, with an error of 1.72%. In addition, the junction temperature swings of the Cauer thermal network model established based on the theoretical calculation and the IR measurement are 15.57 °C and 15.90 °C, respectively, a difference of only 0.33 °C.

Similarly, as shown in Figure 14b, under DC-2 test conditions, the maximum junction temperature calculated by the Cauer thermal network model based on the theoretical calculation is 144.95 °C, which is very close to the maximum junction temperature of 142.24 °C obtained by IR measurement; this temperature represents a difference of approximately 2.71 °C, with an error of 1.91%. In addition, the junction temperature swings of the Cauer thermal network model established based on the theoretical calculation and the IR measurement are 73.71 °C and 78.07 °C, respectively, a difference of only 4.36 °C. The results indicate that the Cauer thermal network model established based on theoretical formulas can accurately predict the maximum and minimum junction temperatures of IGBT chips.

However, unlike the Cauer thermal network model based on theoretical formulas that can obtain a good maximum junction temperature, the maximum junction temperature predicted by the Cauer thermal network model according to the transient thermal impedance curve test and the structure function differs somewhat from the maximum junction temperature obtained by the IR measurement. Under the DC-1 test condition, the maximum junction temperature calculated by the Cauer thermal network model based on the structure function is 58.32 °C, which is approximately 6.79 °C (or nearly 10.43%) different from the maximum junction temperature measured by the IR measurement. Under the DC-2 test condition, the maximum junction temperature calculated by the Cauer thermal network model established based on the structure function is 132.95 °C, which is approximately 9.29 °C (or nearly 6.53%) different from the maximum junction temperature measured by the IR measurement.

The differences in the junction temperature swings are even greater. Under DC-1 conditions, the junction temperature swing calculated by the Cauer thermal network model based on the structure function is 5.78 °C, which is 10.12 °C lower than the junction temperature swing obtained from the IR measurement. Under the DC-2 condition, the calculated junction temperature difference is 49.91 °C lower than that obtained from the IR measurement.

The comparison demonstrates that the junction temperature obtained by the Cauer thermal network model based on the structure function is closer to the IGBT module's junction temperature measured by the TSEP method. The difference is only 1.26 °C under DC-1 test conditions and 2.42 °C under DC-2 test conditions. The results indicate that the temperature predicted by the Cauer thermal network model based on the structure function is closer to the average junction temperature of the IGBT chip, mainly because in obtaining the structure function, the transient thermal impedance curve is calculated using the cooling curve of the IGBT module obtained by the TSEP method. Because the junction temperature obtained from the TSEPs is the average junction temperature, the calculated transient thermal impedance is relatively small. Therefore, the maximum junction temperature obtained by the Cauer thermal network model obtained by the structure function method is lower than the maximum temperature of the IGBT chip and is closer to the average junction temperature of the IGBT chip.

The maximum junction temperature calculated by the Cauer thermal network model based on the theoretical calculation is very close to the maximum junction temperature, while the Cauer thermal network model based on the structure function cannot obtain a good maximum junction temperature. The main reason for this result is that in the process of obtaining the structure function method, the cooling curve of the IGBT module is obtained by the TSEP method, and then the transient thermal impedance curve is calculated. The junction temperature obtained by the TSEP method is the average junction temperature instead of the maximum junction temperature. Therefore, the "maximum junction temperature" obtained by the Cauer thermal network model based on the structure function method is lower than the actual maximum junction temperature at the center of the chip.

6.3. Comparison of the Junction Temperatures Obtained by the FE Analysis and Those Calculated by the RC Thermal Network Models Obtained by the Two Methods

To further analyze the *RC* thermal network models obtained by the two methods, the temperature of each material layer is obtained by FE analysis, and the results are compared with those obtained with the *RC* thermal network model.

Figure 15 shows the profile temperature field distribution of the IGBT module at the moment of power turn-off; the temperatures were obtained by FE analysis. The midpoint of the upper surface of each layer on the thermal path of the IGBT-2 chip is selected as the monitoring point.

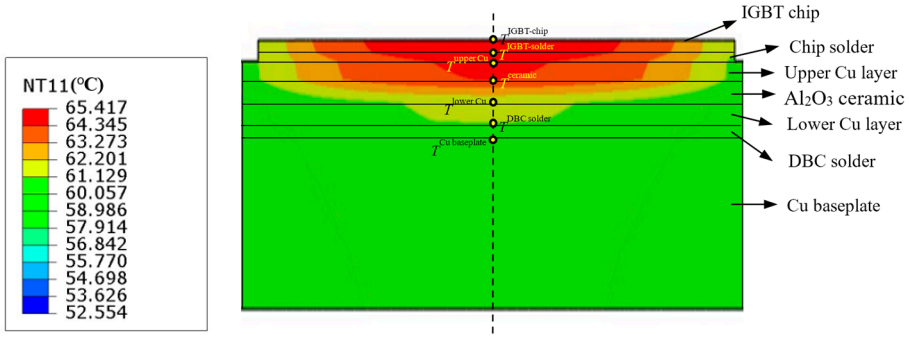


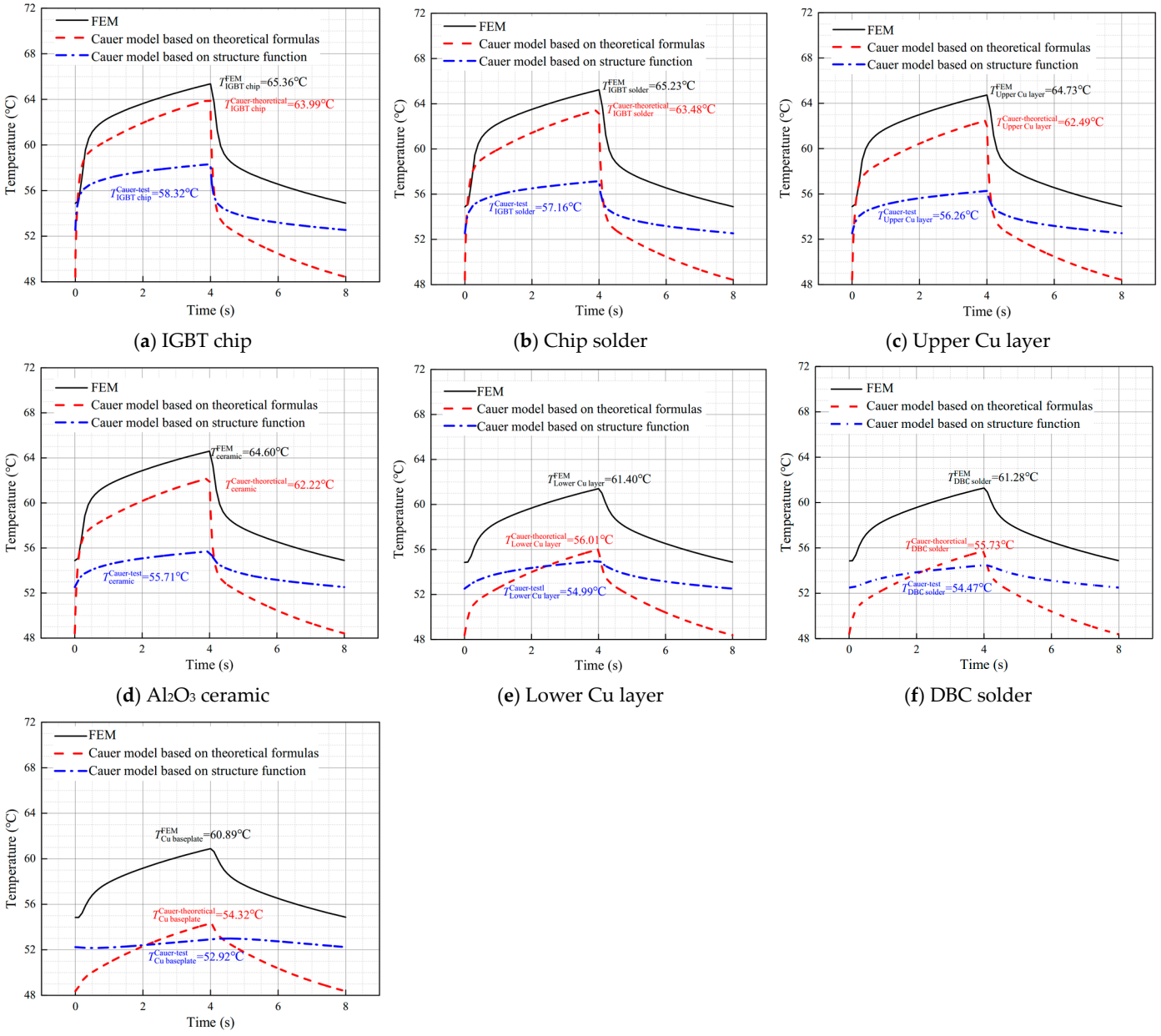
Figure 15. Temperature monitoring points on the IGBT-2 chip heat flow path.

Figure 16 and Table 6 show the comparison results of temperature changes at various monitoring points within one power cycle under DC-1 conditions. The maximum temperatures of the IGBT chip, the chip solder layer, the upper Cu layer, and the ceramic layer calculated by the Cauer thermal network model based on the theoretical calculation accord well with the maximum temperatures obtained from the FE analysis, and the error range is 2.10–3.68%. For the maximum temperatures of the lower Cu layer, the DBC solder layer, and the Cu baseplate, the differences significantly increase compared to the FE results, and the error range is 8.78–10.79%.

Similarly, Figure 17 and Table 7 show the comparison results of temperature changes at various monitoring points within one power cycle under DC-2 conditions. The maximum temperatures of the IGBT chip, the chip solder layer, the upper Cu layer, and the ceramic layer calculated by the Cauer thermal network model established based on the theoretical calculation are very close to the maximum temperatures obtained by the FE analysis, and the error range is 0.60–2.08%. However, the maximum temperatures of the lower Cu layer, the DBC solder layer, and the Cu baseplate differ significantly from those obtained by the FE analysis, and the error range is 10.55–15.93%.

The Cauer thermal network model established based on theoretical formulas can better predict the maximum temperature of material layers close to the IGBT chip, while the prediction results are not ideal for the material layers close to the heat sink because in the FE analysis, the convective heat transfer coefficient is set on the bottom surface of the IGBT module to simulate the water-cooled heat sink in the power cycling test, thus making it difficult for the heat of material layers near the bottom surface of the IGBT module to dissipate, and the temperature remains relatively high. However, in the Cauer thermal network model, a fixed temperature boundary condition is set, and the heat in material layers close to the boundary can therefore be quickly dissipated. Therefore, when comparing the temperatures of the Cauer thermal network model with those determined by the FE analysis, the error of material layers close to the heat sink is relatively large.

Under the DC-1 condition, the error in the material layer temperature obtained by the Cauer thermal network model established based on the structure function is greater than 10%. Under the DC-2 condition, the errors in temperatures obtained for the chip solder layer, the upper Cu layer, and the ceramic layer by the Cauer thermal network model established based on the structure function compared to those obtained by the FE analysis are all greater than 7%, while the errors in temperatures of the lower Cu layer, the DBC solder layer, and the Cu baseplate are reduced; however, the differences in the junction temperature swing are relatively large, and the minimum error of the junction temperature difference is 73.45%. Therefore, the material layer temperature calculated by the Cauer thermal network model based on the structure function has a relatively large error.



(**a**) IGBT chip (**b**) Chip solder (**c**) Upper Cu layer

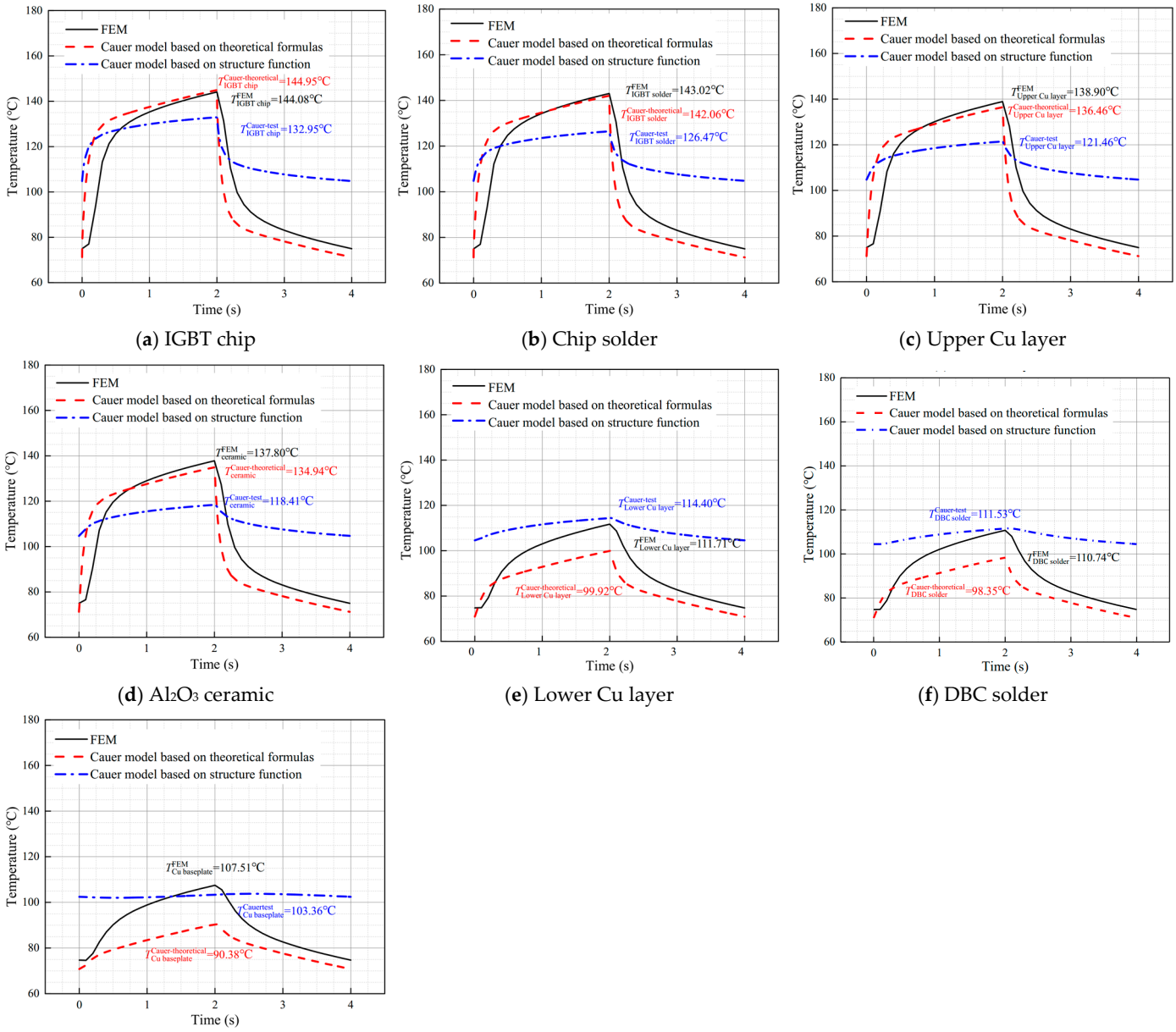
(**d**) Al_2O_3 ceramic (**e**) Lower Cu layer (**f**) DBC solder

(**g**) Cu baseplate

Figure 16. Comparison of the Cauer model calculation results and FE calculation results for each material layer under DC-1 conditions.

Table 6. Verification of the Cauer thermal network models under DC-1 conditions by FE analysis.

Monitoring Point	FE	Cauer-Theoretical Formulas	Error	Cauer-Test	Error
$T^{\text{IGBT chip}}$	65.36	63.99	2.10%	58.32	10.77%
$T^{\text{chip solder}}$	65.23	63.48	2.68	57.16	12.37%
$T^{\text{upper Cu}}$	64.73	62.49	3.46%	56.26	13.09%
T^{ceramics}	64.60	62.22	3.68%	55.71	13.76%
$T^{\text{lower Cu}}$	61.40	56.01	8.78%	54.99	10.44%
$T^{\text{DBC solder}}$	61.28	55.73	9.06%	54.47	11.11%
$T^{\text{Cu baseplate}}$	60.89	54.32	10.79%	52.92	13.09%



(**a**) IGBT chip (**b**) Chip solder (**c**) Upper Cu layer

(**d**) Al_2O_3 ceramic (**e**) Lower Cu layer (**f**) DBC solder

(**g**) Cu baseplate

Figure 17. Comparison of the Cauer model calculation results and FE calculation results for each material layer under DC-2 conditions.

Table 7. Verification of the Cauer thermal network models under DC-2 conditions by FE analysis.

Monitoring Point	FE	Cauer-Theoretical Formulas	Error	Cauer-Test	Error
$T^{\text{IGBT chip}}$	144.08	144.95	0.60%	132.95	7.72%
$T^{\text{chip solder}}$	143.02	142.06	0.67%	126.47	11.57%
$T^{\text{upper Cu}}$	138.90	136.46	1.76%	121.46	12.56
T^{ceramics}	137.80	134.94	2.08%	118.41	14.07%
$T^{\text{lower Cu}}$	111.71	99.92	10.55%	114.40	2.41%
$T^{\text{DBC solder}}$	110.74	98.35	11.19%	111.53	0.71%
$T^{\text{Cu baseplate}}$	107.51	90.38	15.93%	103.36	3.86%

7. Conclusions

In this paper, the thermal parameters of the Cauer thermal network model are obtained by two methods, i.e., theoretical calculation and the experimentally obtained structure function. The junction temperatures calculated by the Cauer thermal network models are compared with the junction temperatures obtained from IR measurements during the power cycling test, the junction temperatures measured by the TSEP method, and the junction temperatures calculated by FE analysis.

For the Cauer thermal network model established based on theoretical formulas, the influence of the lateral and vertical boundary effects on the heat spreading angle is considered, and the parameters of each *RC* unit are obtained according to the structural dimensions and material parameters of each material layer. The junction temperatures calculated by the Cauer thermal network model based on theoretical formulas are very close to the highest and lowest junction temperatures obtained by IR measurement in the power cycling test, and the error of the highest junction temperature is less than 2%. For material layers close to the IGBT chip, e.g., the chip solder layer, the upper Cu layer, and the ceramic layer, the temperatures obtained by the Cauer thermal network model based on theoretical formulas are relatively close to the temperatures obtained by the FE analysis, while for material layers close to the heat sink, there is a certain error. The Cauer thermal network model established based on theoretical formulas can better predict the maximum junction temperature of the IGBT chip and the maximum temperature of the material layers close to the IGBT chip, while for the material layers away from the IGBT chip near the heat sink, the predictions are poor.

For the Cauer thermal network model established by the structure function, the transient thermal impedance curve is obtained based on the thermal resistance experiment by using the TSEP method, and the parameters of each *RC* unit are obtained from the structure function. The junction temperature calculated by the Cauer thermal network model based on the structure function is relatively close to the average junction temperature of the IGBT chip obtained by the TSEP method in the power cycling test. Therefore, the Cauer thermal network model established by the structure function can better predict the average junction temperature of the IGBT chip.

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