Effect of different solder layer damage on junction temperature of IGBT module

Siyuan Song
Institute of Electronics Packaging Technology and Reliability
School of Mathematics,Statistics and Mechanics
Beijing University of Technology
Beijing, China
ssy779@emails.bjut.edu.cn

Tong An*
Institute of Electronics Packaging Technology and Reliability
School of Mathematics,Statistics and Mechanics
Beijing University of Technology
Beijing, China
antong@bjut.edu.cn

Fei Qin
Institute of Electronics Packaging Technology and Reliability
School of Mathematics,Statistics and Mechanics
Beijing University of Technology
Beijing, China
qfei@bjut.edu.cn

Yanpeng Gong
Institute of Electronics Packaging Technology and Reliability
School of Mathematics,Statistics and Mechanics
Beijing University of Technology
Beijing, China
yanpeng.gong@bjut.edu.cn

Yanwei Dai
Institute of Electronics Packaging Technology and Reliability
School of Mathematics,Statistics and Mechanics
Beijing University of Technology
Beijing, China
ywdai@bjut.edu.cn

Pei Chen
Institute of Electronics Packaging Technology and Reliability
School of Mathematics,Statistics and Mechanics
Beijing University of Technology
Beijing, China
peichen@bjut.edu.cn

2024 25th International Conference on Electronic Packaging Technology (ICEPT) | 979-8-3503-5380-8/24/$31.00 ©2024 IEEE | DOI: 10.1109/ICEPT63120.2024.10668476

***Abstract*—During the operation of IGBT (Insulated Gate Bipolar Transistor), the power loss and junction temperature of the IGBT module vary with the usage conditions. This is mainly due to the mismatch in thermal expansion coefficients of different materials, which leads to thermal stress repeatedly acting on the solder layer. As a result, the solder layer may fail. Therefore, investigating solder layer damage is crucial for enhancing the reliability of IGBT modules. In this study, a three-dimensional finite element model of the IGBT module is established. The damage to the solder layer is investigated by simulating the reduction of solder layer area in different regions. Specifically, junction temperature (T_j), and maximum temperature (T_{max}) of various IGBT modules under power cycle conditions are recorded. This is done when the solder layer of the chip and copper baseplate is separately reduced by 10%, and when the areas of both solder layers are simultaneously reduced by 10%. Finally, the effects of solder layer damage in different regions on T_j and T_{max} are analyzed. The results obtained through finite element analysis indicate that T_j and T_{max} reach their maximum values when the areas of both solder layers are decreased simultaneously. Conversely, T_j and T_{max} are minimized when the area of the copper baseplate solder layer is reduced. Moreover, T_j and T_{max} increase as the area of the solder layer decreases.**

Keywords— IGBT; Junction temperature; Solder layer; Finite element model.

I. INTRODUCTION

With the progress of scientific research technology and the improvement of manufacturing process, IGBT module has become a more ideal switching device in the field of power electronics, has replaced the original GTR and part of the power MOSFET market [1] , as the core of the energy conversion system is widely used in the new energy vehicles, rail transportation, smart grid, photovoltaic and wind power industry, etc.

The IGBT module consists of bonding wires, metallization layer, chip, chip solder layer, DBC, copper baseplate solder layer, and copper baseplate. Among them, The chip solder layer is between the chip and the upper copper layer, and the copper baseplate solder layer is between the DBC and the copper baseplate, both have a key role to play in the heat transfer of IGBT modules, and its degree of failure directly affects the degree of aging of the IGBT. This is due to the thermal expansion coefficient of the solder layer adjacent materials differ greatly, and the thermal expansion coefficient of the smaller material for the tensile state, the thermal expansion coefficient of the larger material for the compression state. This causes the stresses in various parts of the module to vary with temperature when the device is heated. With the IGBT working time extension and temperature increase, the solder layer produces cyclic thermal stress, and with the increase in cycle time, the solder layer gradually produce damage, the damage accumulates progressively with the number of cycles, resulting in stress concentration prone to cracking, and in the repeated action of stress cracks will continuously extend, which makes the solder cracking or interface delamination, resulting in the failure of the solder layer, and ultimately lead to the failure of the IGBT module. Therefore, it is of great significance to carry out the research on the damage of solder layer of IGBT module for its reliability.

Literature [2] calculates the solder Anand model parameters and establishes the solder intrinsic model through the results obtained from tensile experiments. The inelastic energy density of solder layers containing different positions of voids, different void percentages, different void types, and different void volume fractions is comparatively analyzed by simulating solder layer voids through the probability law of solder layer voids. Based on the analysis of the results of the inelastic strain energy density, the conclusion was obtained that the solder layer life is related to the statistical distribution of the voids in addition to the size and location of the voids in the weld. Among them, the fatigue life of welded joints is positively correlated with the void volume fraction. Literature [3] in addition to the cavity size, location, but also on the solder layer cavity depth to do the relevant research, the conclusion proves that is located in the contact surface of the cavity than buried in the solder layer under the cavity has a more serious cumulative damage, of which penetrating cavities on the reliability of the module has the greatest impact. In this paper, we will study the effect of the respective damage and common damage of the two solder layers on the T_j of IGBT modules during the service process of IGBT modules. Literature [4] investigated the effects of cavity size, cavity location and solder layer thickness on T_j of IGBT module. Depending on the simulation results of different cavity sizes,

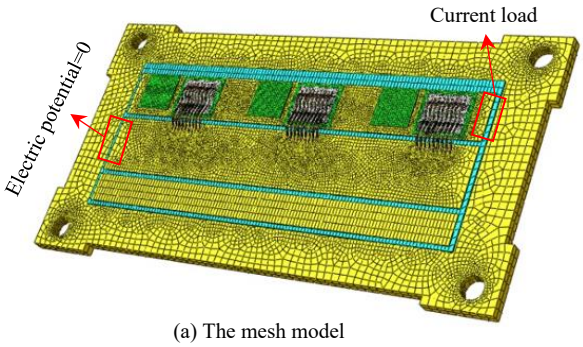
This work was supported in part by the National Natural Science Foundation of China (NSFC), under Grant 12272013.

the positive correlation between the cavity radius and the chip T_j is obtained; the simulation results of different locations of the root cavity are shown to give the conclusion that the cavity at the corner of the solder layer has the greatest influence on the T_j of the IGBT module; and according to the simulation results of the distribution of the cavities, it is obtained that the denser the cavity is, the higher the T_j of the module is, when the cavities are of the same size and are not located at the corners. Literature [5] characterizes the effect of two aging modes, voids and cracks, on module lifetime by using thermal resistance through emulation. In this case, voids have a high effect on heat dissipation, which in turn leads to a fast increasing thermal resistance. Whereas, cracks lead to an enlarged stress around the cracks in the solder layer, which in turn leads to the expansion of the cracks from the periphery to the center, thus affecting the overall lifetime.

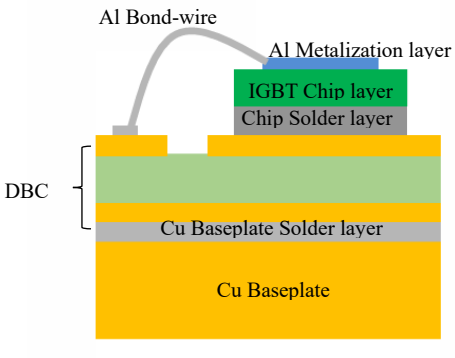
II. FINITE ELEMENT ANALYSIS

A. Finite Element Model and Load

A 3D finite element model of the IGBT module is established when the solder layer is undamaged as shown in Fig. 1. Apply the cyclic current load to the upper side Cu layer 10 times as shown in Fig. 2, with a loading current size of 300 A, and on and off times of ton=2 s and toff=2 s. The potential of the lower side Cu layer is zero. Because IGBT in the power cycle test need to add water-cooled cooling device to help module cooling, the lower surface of the Cu baseplate set convection heat transfer coefficient to simulate water-cooled device, the coefficient is set to 2.9 W/(mm^2·K), the temperature is 45°C. Set the ambient temperature of the entire module to 23°C to simulate the actual working environment of the module.



(a) The mesh model



(b) Schematic cross-section

Fig. 1. The FE model of IGBT (a) The mesh model, (b) Schematic cross-section.

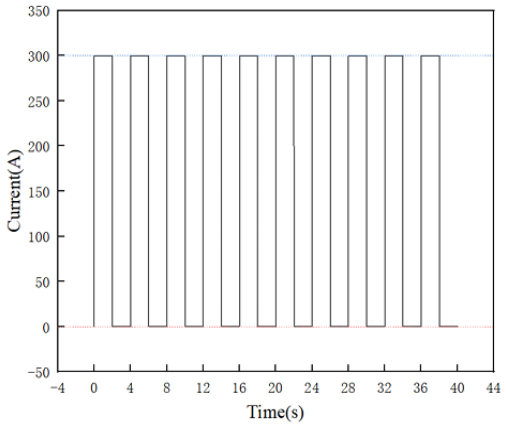


Fig. 2. Cyclic current load with an amplitude of 300 A, a cycle of 4 seconds and a duty ratio of 0.5

TABLE I MATERIAL PROPERIES

Materials	Thermal conduction (W/m·K)	Specific heat (J/(kg·K))	Density (10^{12}kg/mm^3)
Al	237	900	2.70×10^{-9}
Cu	400	380	8.92×10^{-9}
Ceramic	20	735	3.96×10^{-8}
Si Chips	148	700	2.33×10^{-9}
Solser (SAC305)	60	220	7.40×10^{-9}
Solder (SnSb5)	64	220	7.34×10^{-9}

B. Results and Analysis

Thermo-electric power sequential coupling simulation of modules, i.e., electrical-thermal analysis is conducted before loading the temperature field for thermal-force analysis. Both parts of the simulation mesh division are using hexahedral cells, but the cell type selection is not the same, in the electric-thermal choose DC3D8E cell type, while in the thermal - force simulation choose C3D8R cell type. From Figure 3 IGBT module two solder layers stress cloud can be observed solder layer stress concentration distribution in the position of the edge, that is, there is no damage inside the solder layer, the edge of the solder layer is easy to produce damage.

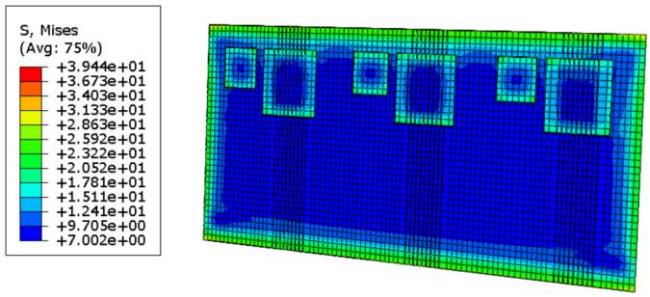
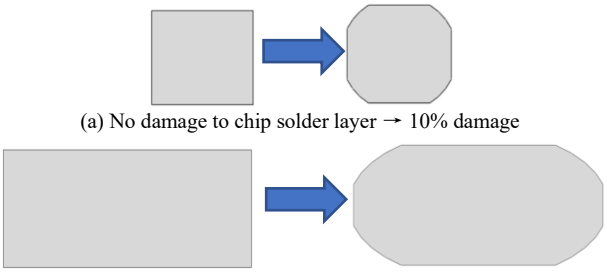


Fig. 3. Stress cloud of IGBT two solder layers.

C. Shape Parameter

Based on the damage-free solder layer thermo-electric coupling stress distribution, the IGBT module solder layer is designed for damage as shown in Fig. 4. MATLAB software was used to write a program to determine the parameters of the solder layer damage model, where a 10% reduction in the solder layer area is 10% solder layer damage. As shown in Table 2, the finite element simulations were divided into four groups for temperature comparison. Set group A for the solder layer without damage, group B for the chip solder layer

damage 10% case, group C for the baseplate solder layer damage 10% case, group D for the overall solder layer damage 10% case.



(a) No damage to chip solder layer → 10% damage

(b) No damage to Cu baseplate solder layer → 10% damage

Fig. 4. Solder layer damage design: (a) chip solder layer no damage → damage 10%; (b) Cu baseplate solder layer no damage → damage 10%.

TABLE II GROUPS AND CHANGING PARAMETERS

Materials	Degree of chip solder layer damage (%)	Degree of Cu baseplate solder layer damage (%)
A	0	0
B	10	0
C	0	10
D	10	10

III. RESULTS AND DISCUSSION

As shown in Fig. 5, the simulation results of different damage locations show that the IGBT module is subjected to different thermal stresses at different damage locations of the solder layer. T_j and T_{max} are the largest when the area of both solder layers decreases at the same time, and T_j and T_{max} are the smallest only when the area of the Cu baseplate solder layer decreases. The effect of the change in the location of the solder layer damage on the junction temperature will be discussed below by comparing the simulation results at the same moment (38th s) for each group.

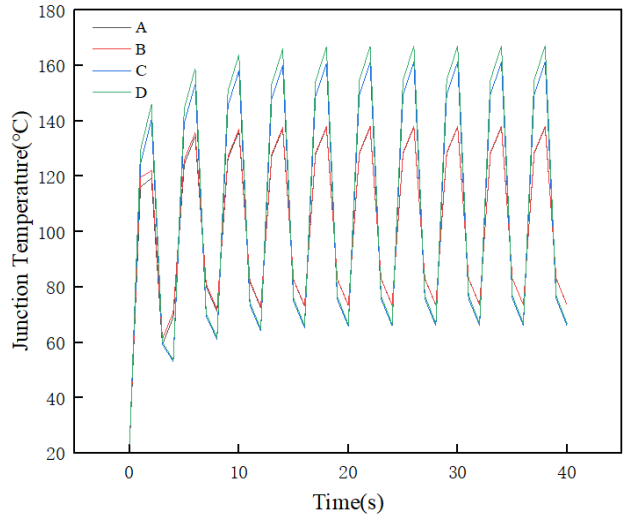


Fig. 5. IGBT module T_j at different damage locations.

A. 10% Chip Solder Layer Damage

When the chip solder layer is damaged by 10%, it can be seen from the T_j cloud diagram in Figure 6 that the high T_j location is concentrated in the upper part of the chip where the metallization layer meets the bonding wires, which will easily trigger the bonding wires to fall off, ultimately leading to the failure of the IGBT module.

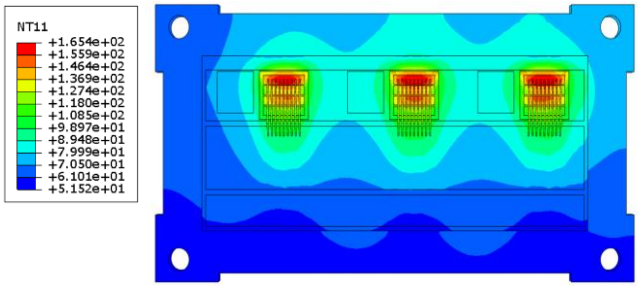


Fig. 6. Cloud view of T_j of IGBT module at 10% damage of chip solder layer

B. 10% Cu Baseplate Solder Layer Damage

When the Cu baseplate solder layer damage 10%, from Figure 7 T_j cloud diagram can be seen, different locations of the chip T_j is different and the high T_j location area is different, the chip 3 is located in the Cu baseplate solder layer damage above the location, as shown in Figure 8, its T_j is the highest.

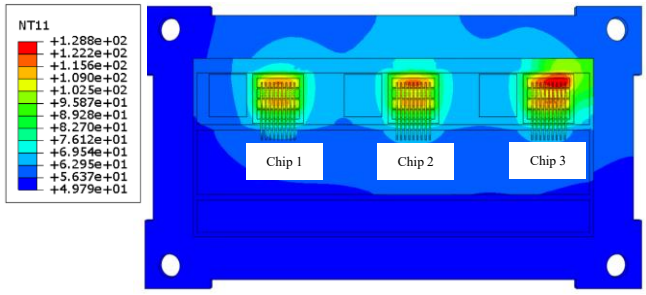


Fig. 7. Cloud view of T_j of IGBT module at 10% damage of copper baseplate solder layer

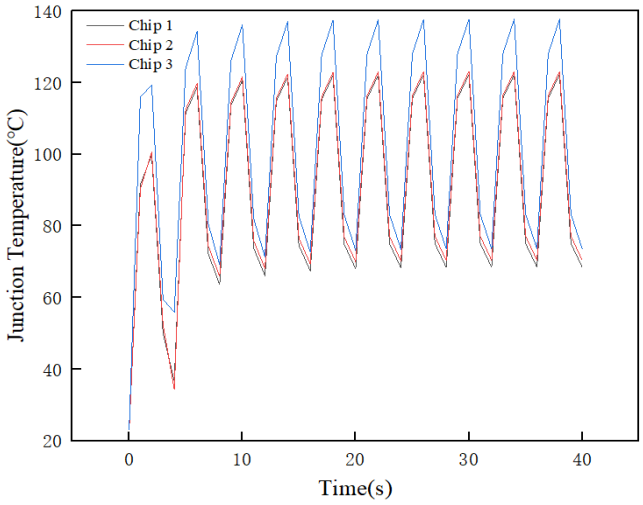


Fig. 8. T_j of the chip at different positions of the IGBT module with 10% damage to the copper baseplate solder layer

C. 10% Overall Solder Layer Damage

At 10% overall solder layer damage, it can be noticed from Fig. 9 that the T_j of the three chips are different depending on the influence of the Cu baseplate solder layer damage.

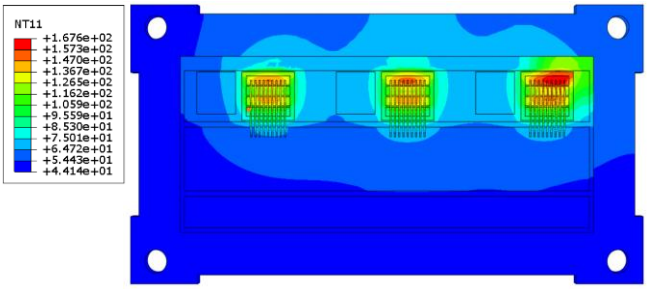


Fig. 9. Cloud view of T_j of IGBT module at 10% damage of overall solder layer

The temperature results as a condition loaded to the overall solder layer damage 10% when the IGBT module mechanical model for thermal coupling analysis, the stress distribution results shown in Figure 10, stress concentration in the solder layer at the upper edge position, and the solder layer has a different degree of warpage, chip 3 below the solder layer warpage is the most serious. This leads to further damage to the solder layer, which accumulates and affects the lifetime of the solder layer, ultimately leading to module failure.

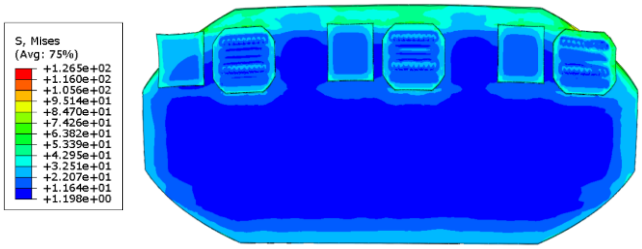


Fig. 10. Cloud view of mises stress of IGBT module at 10% damage of overall solder layer

IV. CONCLUSION

By establishing thermoelectric coupling and thermo-electric coupling models, this paper carries out power cycle simulation for the modules with solder layers located at different damage locations, and obtains the results of the T_j of the chip when the solder layer is damaged at different locations and the results of the maximum stress in the solder layer when the layer is damaged as a whole. Through the analysis, the IGBT module different solder layer damage to the IGBT module T_j impact is different, the overall solder layer are damaged when the T_j is the largest conclusion. And in the case of individual solder layer damage, the chip T_j is higher than the chip T_j when the chip solder layer is damaged than when the Cu baseplate solder layer is damaged. Due to the Cu baseplate solder layer damage will affect the chip T_j, resulting in IGBT module different chip T_j is different, so the actual application process of Cu baseplate solder layer damage can not be ignored.

ACKNOWLEDGMENT

This work was supported in part by the National Natural Science Foundation of China (NSFC), under Grant 12272013.

REFERENCES

[1] Zhou R, An T, Qin F, et al. Influence of chip layout on temperature distribution of multi-chip press pack IGBT devices[C]//2022 23rd International Conference on Electronic Packaging Technology (ICEPT). IEEE, 2022: 1-4.

[2] Le V, Benabou L, Etgens V, et al. Finite element analysis of the effect of process induced voids on the fatigue lifetime of a lead-free solder joint under thermal cycling. Microelectronics Reliability, 2016, 65: 243-254.

[3] Otiaba K C, Okereke M I, Bhatti R S. Numerical assessment of the effect of void morphology on thermo-mechanical performance of solder thermal interface material. Applied Thermal Engineering, 2014,64(1-2): 51-63.

[4] Jiang N, Chen M, Xu S, et al. Lifetime evaluation of solder layer in an IGBT module under different temperature levels[C]//2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia). IEEE, 2016: 3137-3141.

[5] Zhu Q, Chen Q, Zhu L, et al. Aging Failure Analysis of IGBT Module Solder Layer Based on Multi-physical Field Coupling[C]//2023 5th Asia Energy and Electrical Engineering Symposium (AEEES). IEEE, 2023: 401-405.